FEATURES

ARM720T Processor
- — ARM7TDMI CPU
- — 8 KB of four-way set-associative cache
- — MMU with 64-entry TLB
- — Thumb code support enabled

Ultra low power
- — 90 mW at 74 MHz typical
- — 30 mW at 18 MHz typical
- — 10 mW in the Idle State
- — <1 mW in the Standby State

48 KB of on-chip SRAM

MaverickKey™ IDs
- — 32-bit unique ID can be used for SDMI compliance
- — 128-bit random ID

Dynamically programmable clock speeds of 18, 36, 49, and 74 MHz

High-performance, Low-power, System-on-chip with SDRAM & Enhanced Digital Audio Interface

OVERVIEW

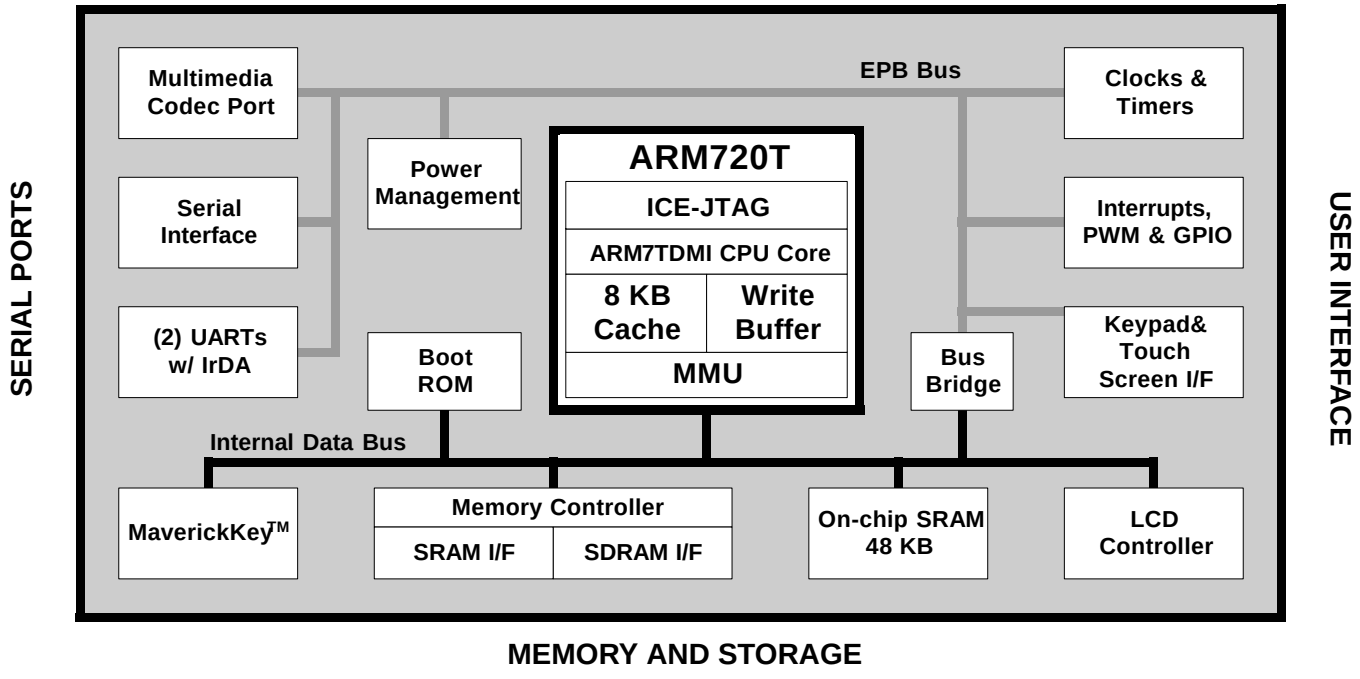
The Maverick™ EP7311 is designed for ultra-low-power applications such as PDAs, smart cellular phones, and industrial hand held information appliances. The core-logic functionality of the device is built around an ARM720T processor with 8 KB of four-way set-associative unified cache and a write buffer. Incorporated into the ARM720T is an enhanced memory management unit (MMU) which allows for support of sophisticated operating systems like Linux®.

Plays Windows® Media

(cont.)

(cont.)

BLOCK DIAGRAM



FEATURES *(cont)*

LCD controller

— Interfaces directly to a single-scan panel monochrome STN LCD

— Interfaces to a single-scan panel color STN LCD with minimal external glue logic

Full JTAG boundary scan and Embedded ICE® support

Integrated Peripheral Interfaces

— 32-bit SDRAM Interface up to 2 external banks

— 8/32/16-bit SRAM/FLASH/ROM Interface

— Multimedia Codec Port

— Two Synchronous Serial Interfaces (SSI1, SSI2)

— CODEC Sound Interface

— 8×8 Keypad Scanner

— 27 General Purpose Input/Output pins

— Dedicated LED flasher pin from the RTC

Internal Peripherals

— Two 16550 compatible UARTs

— IrDA Interface

— Two PWM Interfaces

— Real-time Clock

— Two general purpose 16-bit timers

— Interrupt Controller

— Boot ROM

Package

— 256-Ball PBGA

The fully static EP7311 is optimized for low power dissipation and is fabricated on a 0.25 micron CMOS process

Development Kits

— EDB7312: Development Kit with color STN LCD on board.

*Note: * Use the EDB7312 Development Kit for all the EP73xx devices.*

OVERVIEW *(cont.)*

The EP7311 is designed for low-power operation. Its core operates at only 2.5 V, while its I/O has an operation range of 2.5 V–3.3 V. The device has three basic power states: operating, idle and standby.

One of its notable features is MaverickKey unique IDs. These are factory programmed IDs in response to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs consist of two registers, one 32-bit series register and one random 128-bit register that may be used by an OEM for an authentication mechanism.

Simply by adding desired memory and peripherals to the highly integrated EP7311 completes a low-power system solution. All necessary interface logic is integrated on-chip.

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Processor Core - ARM720T

The EP7311 incorporates an ARM 32-bit RISC microcontroller that controls a wide range of on-chip peripherals. The processor utilizes a three-stage pipeline consisting of fetch, decode and execute stages. Key features include:

- ARM (32-bit) and Thumb (16-bit compressed) instruction sets
- Enhanced MMU for Microsoft Windows CE and other operating systems
- 8 KB of 4-way set-associative cache.
- Translation Look Aside Buffers with 64 Translated Entries

Power Management

The EP7311 is designed for ultra-low-power operation. Its core operates at only 2.5 V, while its I/O has an operation range of 2.5 V–3.3 V allowing the device to achieve a performance level equivalent to 60 MIPS. The device has three basic power states:

- Operating — This state is the full performance state. All the clocks and peripheral logic are enabled.
- Idle — This state is the same as the Operating State, except the CPU clock is halted while waiting for an event such as a key press.
- Standby — This state is equivalent to the computer being switched off (no display), and the main oscillator shut down. An event such as a key press can wake-up the processor.

Pin Mnemonic	I/O	Pin Description
BATOK	I	Battery ok input
nEXTPWR	I	External power supply sense input
nPWRFL	I	Power fail sense input
nBATCHG	I	Battery changed sense input

Table A. Power Management Pin Assignments

MaverickKey™ Unique ID

MaverickKey unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

Both a specific 32-bit ID as well as a 128-bit random ID is programmed into the EP7311 through the use of laser probing technology. These IDs can then be used to match secure copyrighted content with the ID of the target device the EP7311 is powering, and then deliver the copyrighted information over a secure connection. In addition, secure transactions can benefit by also matching device IDs to server IDs. MaverickKey IDs provide a level of hardware security required for today's Internet appliances.

Memory Interfaces

There are two main external memory interfaces. The first one is the ROM/SRAM/FLASH-style interface that has programmable wait-state timings and includes burst-mode capability, with six chip selects decoding six 256 MB sections of addressable space. For maximum flexibility, each bank can be specified to be 8-, 16-, or 32-bits wide. This allows the use of 8-bit-wide boot ROM options to minimize overall system cost. The on-chip boot ROM can be used in product manufacturing to serially download system code into system FLASH memory. To further minimize system memory requirements and cost, the ARM Thumb instruction set is supported, providing for the use of high-speed 32-bit operations in 16-bit op-codes and yielding industry-leading code density.

Pin Mnemonic		I/O	Pin Description
nCS[5:0]		O	Chip select out
A[27:0]		O	Address output
D[31:0]		I/O	Data I/O
nMOE/nSDCAS	(Note)	O	ROM expansion OP enable
nMWE/nSDWE	(Note)	O	ROM expansion write enable
HALFWORD		O	Halfword access select output
WORD		O	Word access select output
WRITE/nSDRAS	(Note)	O	Transfer direction

Table B. Static Memory Interface Pin Assignments

Note: Pins are multiplexed. See Table S on page 11 for more information.

The second is the programmable 16- or 32-bit-wide SDRAM interface that allows direct connection of up to two banks of SDRAM, totaling 512 Mb. To assure the lowest possible power consumption, the EP7311 supports self-refresh SDRAMs, which are placed in a low-power state by the device when it enters the low-power Standby State.

Pin Mnemonic	I/O	Pin Description
SDCLK	O	SDRAM clock output
SDCKE	O	SDRAM clock enable output
nSDCS[1:0]	O	SDRAM chip select out
WRITE/nSDRAS (Note 2)	O	SDRAM RAS signal output
nMOE/nSDCAS (Note 2)	O	SDRAM CAS control signal
nMWE/nSDWE (Note 2)	O	SDRAM write enable control signal
A[27:15]/DRA[0:12] (Note 1)	O	SDRAM address
A[14:13]/DRA[12:14]	O	SDRAM internal bank select
PD[7:6]/SDQM[1:0] (Note 2)	I/O	SDRAM byte lane mask
SDQM[3:2]	O	SDRAM byte lane mask
D[31:0]	I/O	Data I/O

Table C. SDRAM Interface Pin Assignments

Note: 1. Pins A[27:13] map to DRA[0:14] respectively. (i.e. A[27}/DRA[0}, A[26}/DRA[1], etc.) This is to balance the load for large memory systems.
2. Pins are multiplexed. See Table S on page 11 for more information.

Digital Audio Capability

The EP7311 uses its powerful 32-bit RISC processing engine to implement audio decompression algorithms in software. The nature of the on-board RISC processor, and the availability of efficient C-compilers and other software development tools, ensures that a wide range of audio decompression algorithms can easily be ported to and run on the EP7311

Universal Asynchronous Receiver/Transmitters (UARTs)

The EP7311 includes two 16550-type UARTs for RS-232 serial communications, both of which have two 16-byte FIFOs for receiving and transmitting data. The UARTs support bit rates up to 115.2 kbps. An IrDA SIR protocol encoder/decoder can be optionally switched into the RX/TX signals to/from UART 1 to enable these signals to drive an infrared communication interface directly.

Pin Mnemonic	I/O	Pin Description
TXD[1]	O	UART 1 transmit
RXD[1]	I	UART 1 receive
CTS	I	UART 1 clear to send
DCD	I	UART 1 data carrier detect
DSR	I	UART 1 data set ready
TXD[2]	O	UART 2 transmit
RXD[2]	I	UART 2 receive
LEDDRV	O	Infrared LED drive output
PHDIN	I	Photo diode input

Table D. Universal Asynchronous Receiver/Transmitters Pin Assignments

Multimedia Codec Port (MCP)

The Multimedia Codec Port provides access to an audio codec, a telecom codec, a touchscreen interface, four general purpose analog-to-digital converter inputs, and ten programmable digital I/O lines.

Pin Mnemonic	I/O	Pin Description
SIBCLK	O	Serial bit clock
SIBDOUT	O	Serial data out
SIBDIN	I	Serial data in
SIBSYNC	O	Sample clock

Table E. MCP Interface Pin Assignments

Note: See Table R on page 11 for information on pin multiplexes.

CODEC Interface

The EP7311 includes an interface to telephony-type CODECs for easy integration into voice-over-IP and other voice communications systems. The CODEC interface is multiplexed to the same pins as the MCP and SSI2.

Pin Mnemonic	I/O	Pin Description
PCMCLK	O	Serial bit clock
PCMOUT	O	Serial data out
PCMIN	I	Serial data in
PCMSYNC	O	Frame sync

Table F. CODEC Interface Pin Assignments

Note: See Table R on page 11 for information on pin multiplexes.

SSI2 Interface

An additional SPI/Microwire1-compatible interface is available for both master and slave mode communications. The SSI2 unit shares the same pins as the MCP and CODEC interfaces through a multiplexer.

- Synchronous clock speeds of up to 512 kHz
- Separate 16 entry TX and RX half-word wide FIFOs
- Half empty/full interrupts for FIFOs
- Separate RX and TX frame sync signals for asymmetric traffic

Pin Mnemonic	I/O	Pin Description
SSICLK	I/O	Serial bit clock
SSITXDA	O	Serial data out
SSIRXDA	I	Serial data in
SSITXFR	I/O	Transmit frame sync
SSIRXFR	I/O	Receive frame sync

Table G. SSI2 Interface Pin Assignments

Note: See Table R on page 11 for information on pin multiplexes.

Synchronous Serial Interface

- ADC (SSI) Interface: Master mode only; SPI and Microwire1-compatible (128 kbps operation)
- Selectable serial clock polarity

Pin Mnemonic	I/O	Pin Description
ADCLK	O	SSI1 ADC serial clock
ADCIN	I	SSI1 ADC serial input
ADCOUT	O	SSI1 ADC serial output
nADCCS	O	SSI1 ADC chip select
SMPCLK	O	SSI1 ADC sample clock

Table H. Serial Interface Pin Assignments

LCD Controller

A DMA address generator is provided that fetches video display data for the LCD controller from memory. The display frame buffer start address is programmable, allowing the LCD frame buffer to be in SDRAM, internal SRAM or external SRAM.

- Interfaces directly to a single-scan panel monochrome STN LCD
- Interfaces to a single-scan panel color STN LCD with minimal external glue logic
- Panel width size is programmable from 32 to 1024 pixels in 16-pixel increments
- Video frame buffer size programmable up to 128 KB
- Bits per pixel of 1, 2, or 4 bits

Pin Mnemonic	I/O	Pin Description
CL1	O	LCD line clock
CL2	O	LCD pixel clock out
DD[3:0]	O	LCD serial display data bus
FRM	O	LCD frame synchronization pulse
M	O	LCD AC bias drive

Table I. LCD Interface Pin Assignments

64-Keypad Interface

Matrix keyboards and keypads can be easily read by the EP7311. A dedicated 8-bit column driver output generates strobes for each keyboard column signal. The pins of Port A, when configured as inputs, can be selectively OR'ed together to provide a keyboard interrupt that is capable of waking the system from a STANDBY or IDLE state.

- Column outputs can be individually set high with the remaining bits left at high-impedance
- Column outputs can be driven all-low, all-high, or all-high-impedance
- Keyboard interrupt driven by OR'ing together all Port A bits
- Keyboard interrupt can be used to wake up the system
- 8×8 keyboard matrix usable with no external logic, extra keys can be added with minimal glue logic

Pin Mnemonic	I/O	Pin Description
COL[7:0]	O	Keyboard scanner column drive

Table J. Keypad Interface Pin Assignments

Interrupt Controller

When unexpected events arise during the execution of a program (i.e., interrupt or memory fault) an exception is usually generated. When these exceptions occur at the same time, a fixed priority system determines the order in which they are handled. The EP7311 interrupt controller has two interrupt types: interrupt request (IRQ) and fast interrupt request (FIQ). The interrupt controller has the ability to control interrupts from 22 different FIQ and IRQ sources.

- Supports 22 interrupts from a variety of sources (such as UARTs, SSI1, and key matrix.)
- Routes interrupt sources to the ARM720T's IRQ or FIQ (Fast IRQ) inputs
- Five dedicated off-chip interrupt lines operate as level sensitive interrupts

.

Pin Mnemonic	I/O	Pin Description
nEINT[2:1]	I	External interrupt
EINT[3]	I	External interrupt
nEXTFIQ	I	External Fast Interrupt input
nMEDCHG/nBROM (Note)	I	Media change interrupt input

Table K. Interrupt Controller Pin Assignments

Note: Pins are multiplexed. See Table S on page 11 for more information.

Real-Time Clock

The EP7311 contains a 32-bit Real Time Clock (RTC) that can be written to and read from in the same manner as the timer counters. It also contains a 32-bit output match register which can be programmed to generate an interrupt.

- Driven by an external 32.768 kHz crystal oscillator

Pin Mnemonic	Pin Description
RTCIN	Real-Time Clock Oscillator Input
RTCOUT	Real-Time Clock Oscillator Output
VDDRTC	Real-Time Clock Oscillator Power
VSSRTC	Real-Time Clock Oscillator Ground

Table L. Real-Time Clock Pin Assignments

PLL and Clocking

- Processor and Peripheral Clocks operate from a single 3.6864 MHz crystal or external 13 MHz clock
- Programmable clock speeds allow the peripheral bus to run at 18 MHz when the processor is set to 18 MHz and at 36 MHz when the processor is set to 36, 49 or 74 MHz

Pin Mnemonic	Pin Description
MOSCIN	Main Oscillator Input
MOSCOUT	Main Oscillator Output
VDDOSC	Main Oscillator Power
VSSOSC	Main Oscillator Ground

Table M. PLL and Clocking Pin Assignments

DC-to-DC converter interface (PWM)

- Provides two 96 kHz clock outputs with programmable duty ratio (from 1-in-16 to 15-in-16) that can be used to drive a positive or negative DC to DC converter

Pin Mnemonic	I/O	Pin Description
DRIVE[1:0]	I/O	PWM drive output
FB[1:0]	I	PWM feedback input

Table N. DC-to-DC Converter Interface Pin Assignments

Timers

- Internal (RTC) timer
- Two internal 16-bit programmable hardware count-down timers

General Purpose Input/Output (GPIO)

- Three 8-bit and one 3-bit GPIO ports
- Supports scanning keyboard matrix

Pin Mnemonic		I/O	Pin Description
PA[7:0]		I/O	GPIO port A
PB[7:0]		I/O	GPIO port B
PD[0]/LEDFLSH	(Note)	I/O	GPIO port D
PD[5:1]		I/O	GPIO port D
PD[7:6]/SDQM[1:0]	(Note)	I/O	GPIO port D
PE[1:0]/BOOTSEL[1:0]	(Note)	I/O	GPIO port E
PE[2]/CLKSEL	(Note)	I/O	GPIO port E

Table O. General Purpose Input/Output Pin Assignments

Note: Pins are multiplexed. See Table S on page 11 for more information.

Hardware debug Interface

- Full JTAG boundary scan and Embedded ICE® support

Pin Mnemonic	I/O	Pin Description
TCLK	I	JTAG clock
TDI	I	JTAG data input
TDO	O	JTAG data output
nTRST	I	JTAG async reset input
TMS	I	JTAG mode select

Table P. Hardware Debug Interface Pin Assignments

LED Flasher

A dedicated LED flasher module can be used to generate a low frequency signal on Port D pin 0 for the purpose of blinking an LED without CPU intervention. The LED flasher feature is ideal as a visual annunciator in battery powered applications, such as a voice mail indicator on a portable phone or an appointment reminder on a PDA.

- Software adjustable flash period and duty cycle
- Operates from 32 kHz RTC clock
- Will continue to flash in IDLE and STANDBY states
- 4 mA drive current

Pin Mnemonic		I/O	Pin Description
PD[0]/LEDFLSH	(Note)	O	LED flasher driver

Table Q. LED Flasher Pin Assignments

Note: Pins are multiplexed. See Table S on page 11 for more information.

Internal Boot ROM

The internal 128 byte Boot ROM facilitates download of saved code to the on-board SRAM/FLASH.

Packaging

The EP7311 is available in a 208-pin LQFP package, 256-ball PBGA package or a 204-ball TFBGA package.

Pin Multiplexing

The following table shows the pin multiplexing of the MCP, SSI2 and the CODEC. The selection between SSI2 and the CODEC is controlled by the state of the SERSEL bit in SYSCON2. The choice between the SSI2, CODEC, and the MCP is controlled by the MCPSEL bit in SYSCON3 (see the EP73xx User's Manual for more information).

Pin Mnemonic	I/O	MCP	SSI2	CODEC
SSICLK	I/O	SIBCLK	SSICLK	PCMCLK
SSITXDA	O	SIBDOUT	SSITXDA	PCMOUT
SSIRXDA	I	SIBDIN	SSIRXDA	PCMIN
SSITXFR	I/O	SIBSYNC	SSITXFR	PCMSYNC
SSIRXFR	I	p/u	SSIRXFR	p/u
BUZ	O			

Table R. MCP/SSI2/CODEC Pin Multiplexing

The following table shows the pins that have been multiplexed in the EP7311.

Signal	Block	Signal	Block
nMOE	Static Memory	nSDCAS	SDRAM
nMWE	Static Memory	nSDWE	SDRAM
WRITE	Static Memory	nSDRAS	SDRAM
A[27:15]	Static Memory	DRA[0:12]	SDRAM
A[14:13]	Static Memory	DRA[13:14]	SDRAM
PD[7:6]	GPIO	SDQM[1:0]	SDRAM
RUN	System Configuration	CLKEN	System Configuration
nMEDCHG	Interrupt Controller	nBROM	Boot ROM select
PD[0]	GPIO	LEDFLSH	LED Flasher
PE[1:0]	GPIO	BOOTSEL[1:0]	System Configuration
PE[2]	GPIO	CLKSEL	System Configuration

Table S. Pin Multiplexing

System Design

As shown in system block diagram, simply adding desired memory and peripherals to the highly integrated EP7311 completes a low-power system solution. All necessary interface logic is integrated on-chip.

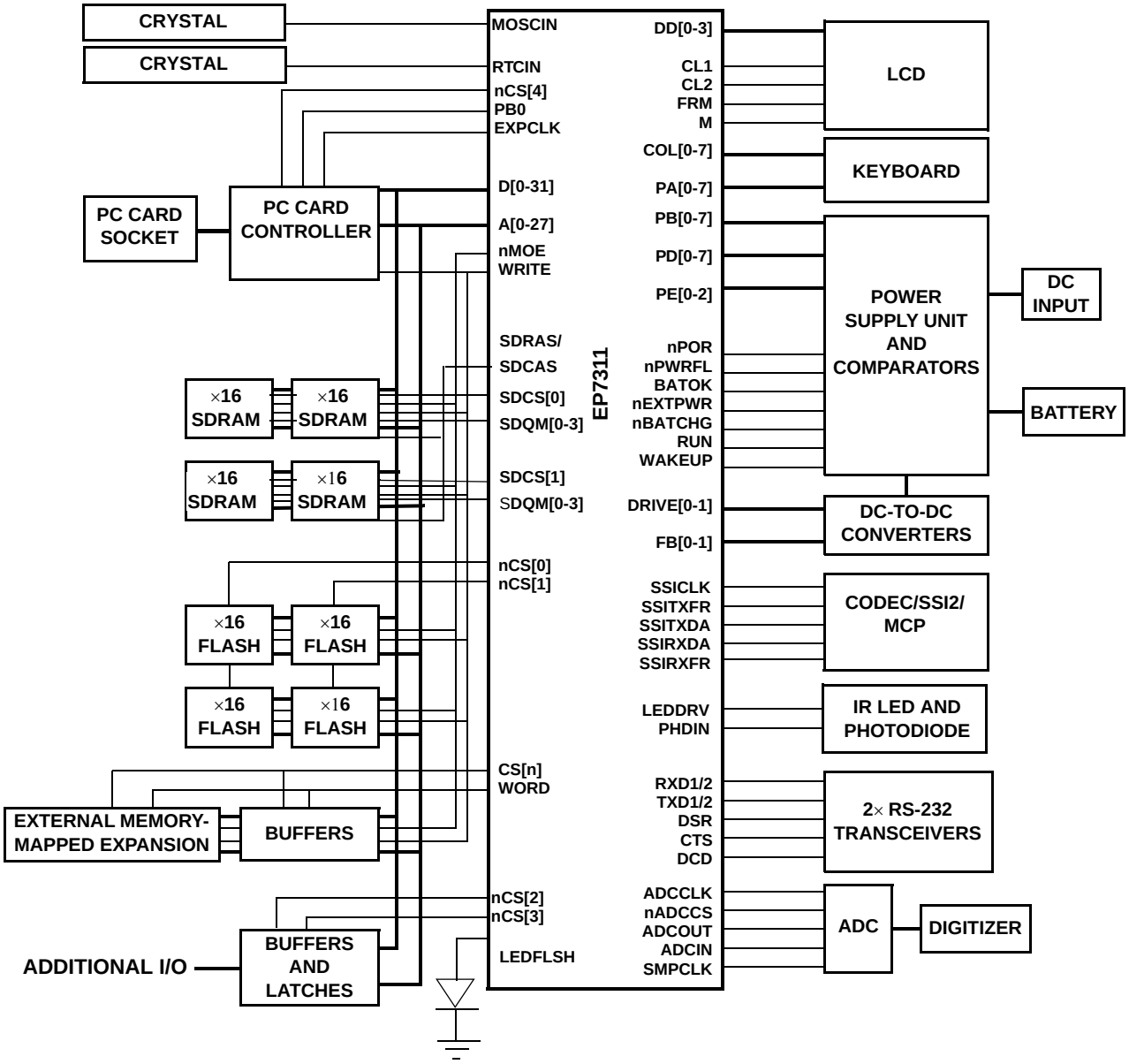


Figure 1. A Maximum EP7311 Based System

Note: A system can only use one of the following peripheral interfaces at any given time: SSI2,CODEC or MCP.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

DC Core, PLL, and RTC Supply Voltage	2.9 V
DC I/O Supply Voltage (Pad Ring)	3.6 V
DC Pad Input Current	±10 mA/pin; ±100 mA cumulative
Storage Temperature, No Power	–40°C to +125°C

Recommended Operating Conditions

DC core, PLL, and RTC Supply Voltage	2.5 V ± 0.2 V
DC I/O Supply Voltage (Pad Ring)	2.3 V - 3.5 V
DC Input / Output Voltage	O–I/O supply voltage
Operating Temperature	Extended -20°C to +70°C; Commercial 0°C to +70°C; Industrial -40°C to +85°C

DC Characteristics

All characteristics are specified at V_{DDCORE} = 2.5 V, V_{DDIO} = 3.3 V and V_{SS} = 0 V over an operating temperature of 0°C to +70°C for all frequencies of operation. The current consumption figures have test conditions specified per parameter."

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VIH	CMOS input high voltage	$0.65 \times V_{DDIO}$	-	V_{DDIO} + 0.3	V	V_{DDIO} = 2.5 V
VIL	CMOS input low voltage	V_{SS} – 0.3	-	$0.25 \times V_{DDIO}$	V	V_{DDIO} = 2.5 V
VT+	Schmitt trigger positive going threshold	-	-	2.1	V	
VT-	Schmitt trigger negative going threshold	0.8	-	-	V	
Vhst	Schmitt trigger hysteresis	0.1	-	0.4	V	VIL to VIH
VOH	CMOS output high voltage[a] Output drive 1[a] Output drive 2[a]	V_{DD} – 0.2 2.5 2.5	- - -	- - -	V V V	IOH = 0.1 mA IOH = 4 mA IOH = 12 mA
VOL	CMOS output low voltage[a] Output drive 1[a] Output drive 2[a]	- - -	- - -	0.3 0.5 0.5	V V V	IOL = –0.1 mA IOL = –4 mA IOL = –12 mA
IIN	Input leakage current	-	-	1.0	µA	VIN = V_{DD} or GND
IOZ	Bidirectional 3-state leakage current[b c]	25	-	100	µA	VOUT = V_{DD} or GND
CIN	Input capacitance	8	-	10.0	pF	
COUT	Output capacitance	8	-	10.0	pF	

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CI/O	Transceiver capacitance	8	-	10.0	pF	
$IDD_{STANDBY}$ @ 25 C	Standby current consumption[1] Core, Osc, RTC @2.5 V I/O @ 3.3 V	 - -	 77 41	 - -	µA	Only nPOR, nPWRFAIL, nURESET, PE0, PE1, and RTS are driven, while all other float, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
$IDD_{STANDBY}$ @ 70 C	Standby current consumption[1] Core, Osc, RTC @2.5 V I/O @ 3.3 V	 - -	 - -	 570 111	µA	Only nPOR, nPWRFAIL, nURESET, PE0, PE1, and RTS are driven, while all other float, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
$IDD_{STANDBY}$ @ 85 C	Standby current consumption[1] Core, Osc, RTC @2.5 V I/O @ 3.3 V	 - -	 - -	 1693 163	µA	Only nPOR, nPWRFAIL, nURESET, PE0, PE1, and RTS are driven, while all other float, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
IDD_{idle} at 74 MHz	Idle current consumption[1] Core, Osc, RTC @2.5 V I/O @ 3.3 V	 - -	 6 10	 - -	mA	Both oscillators running, CPU static, Cache enabled, LCD disabled, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
$VDD_{STANDBY}$	Standby supply voltage	2.0	-	-	V	Minimum standby voltage for state retention, internal SRAM cache, and RTC operation only

a. Refer to the strength column in the pin assignment tables for all package types.

b. Assumes buffer has no pull-up or pull-down resistors.

c. The leakage value given assumes that the pin is configured as an input pin but is not currently being driven.

Note: 1) Total power consumption = IDD_{CORE} x 2.5 V + IDD_{IO} x 3.3 V

2) A typical design will provide 3.3 V to the I/O supply (i.e., V_{DDIO}), and 2.5 V to the remaining logic. This is to allow the I/O to be compatible with 3.3 V powered external logic (i.e., 3.3 V SDRAMs).

2) Pull-up current = 50 µA typical at V_{DD} = 3.3 V.

Timings

Timing Diagram Conventions

This data sheet contains timing diagrams. The following key explains the components used in these diagrams. Any variations are clearly labelled when they occur. Therefore, no additional meaning should be attached unless specifically stated.

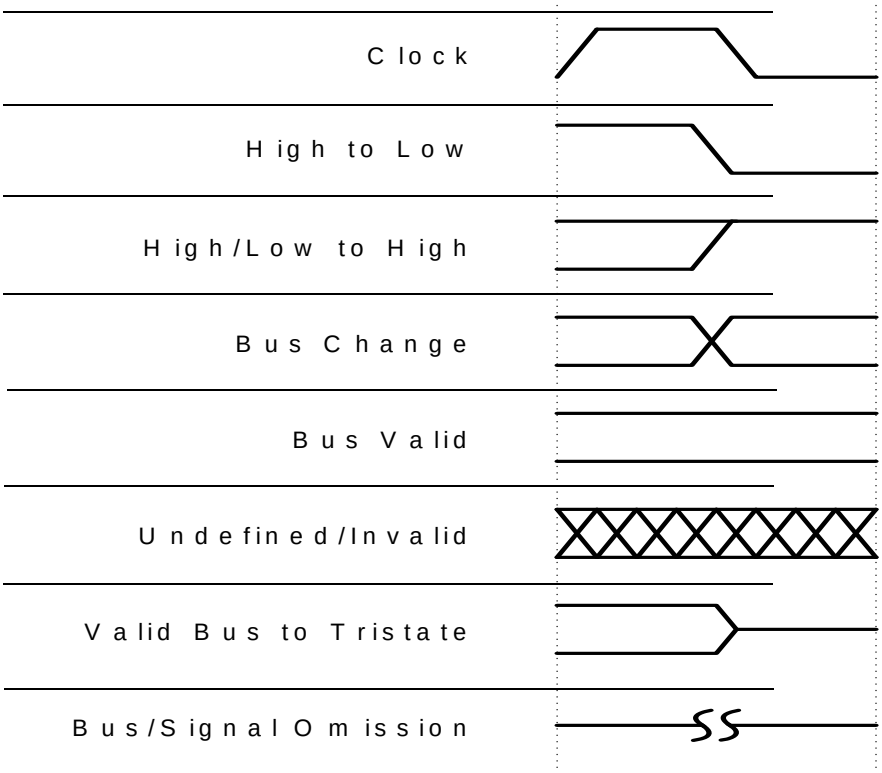


Figure 2. Legend for Timing Diagrams

Timing Conditions

Unless specified otherwise, the following conditions are true for all timing measurements. All characteristics are specified at V_{DDIO} = 3.1 - 3.5 V and V_{SS} = 0 V over an operating temperature of -40°C to +85°C. Pin loadings is 50 pF. The timing values are referenced to 1/2 V_{DD}.

SDRAM Interface

Figure 3 through Figure 6 define the timings associated with all phases of the SDRAM. The following table contains the values for the timings of each of the SDRAM modes.

Parameter	Symbol	Min	Typ	Max	Unit
SDCLK rising edge to SDCS assert delay time	t_{CSa}	0	2	4	ns
SDCLK rising edge to SDCS deassert delay time	t_{CSd}	– 3	2	10	ns
SDCLK rising edge to SDRAS assert delay time	t_{RAa}	1	3	7	ns
SDCLK rising edge to SDRAS deassert delay time	t_{RAd}	– 3	1	10	ns
SDCLK rising edge to SDRAS invalid delay time	t_{RAnv}	2	4	7	ns
SDCLK rising edge to SDCAS assert delay time	t_{CAa}	– 2	2	5	ns
SDCLK rising edge to SDCAS deassert delay time	t_{CAd}	– 5	0	3	ns
SDCLK rising edge to ADDR transition time	t_{ADv}	– 3	1	5	ns
SDCLK rising edge to ADDR invalid delay time	t_{ADx}	– 2	2	5	ns
SDCLK rising edge to SDMWE assert delay time	t_{MWa}	– 3	1	5	ns
SDCLK rising edge to SDMWE deassert delay time	t_{MWd}	– 4	0	4	ns
DATA transition to SDCLK rising edge time	t_{DAs}	2	-	-	ns
SDCLK rising edge to DATA transition hold time	t_{DAh}	1	-	-	ns
SDCLK rising edge to DATA transition delay time	t_{DAd}	0	-	15	ns

SDRAM Load Mode Register Cycle

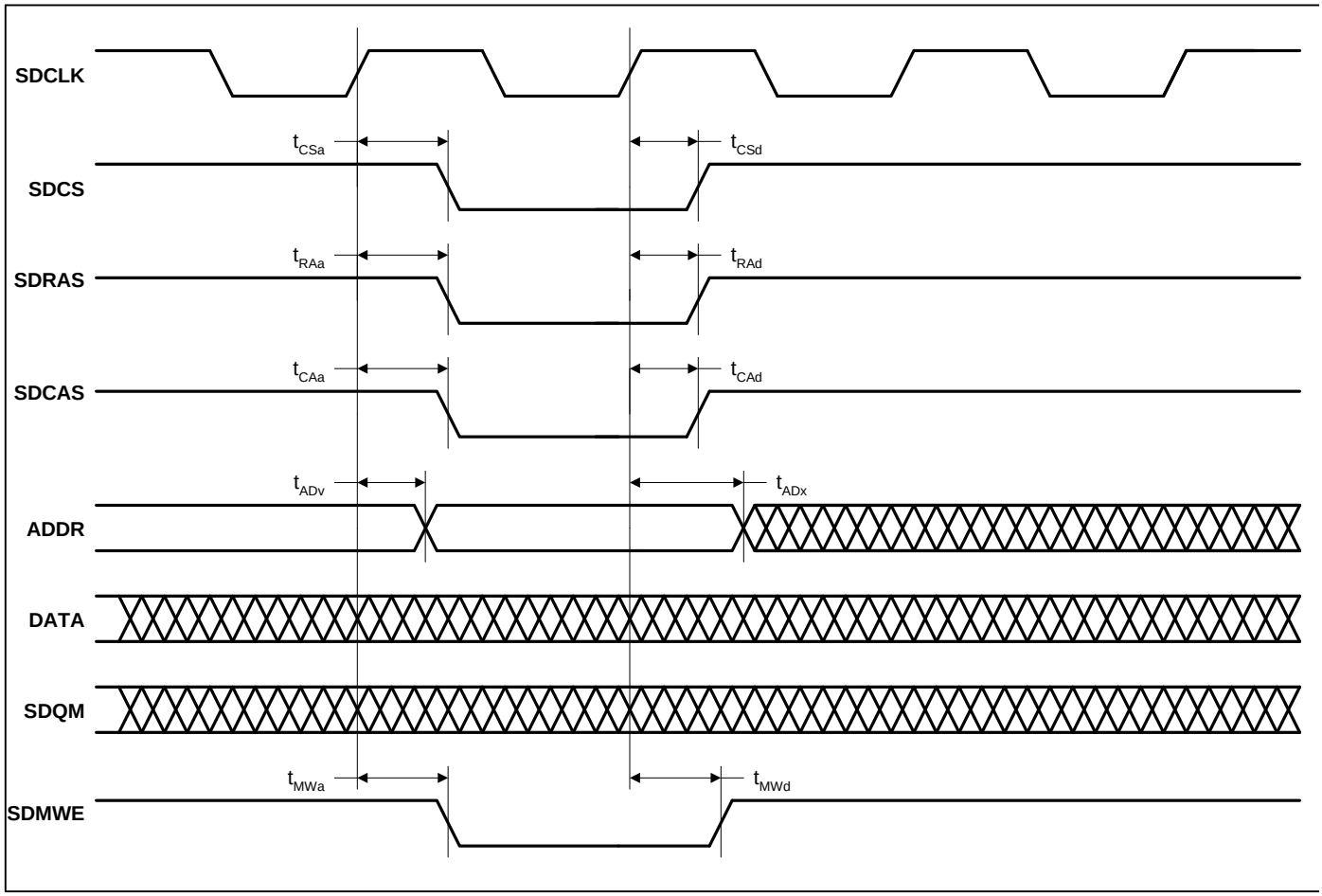


Figure 3. SDRAM Load Mode Register Cycle Timing Measurement

Note: 1. Timings are shown with CAS latency = 2
2. The SDCLK signal may be phase shifted relative to the rest of the SDRAM control and data signals due to uneven loading. Designers should take care to ensure that delays between SDRAM control and data signals are approximately equal

SDRAM Burst Read Cycle

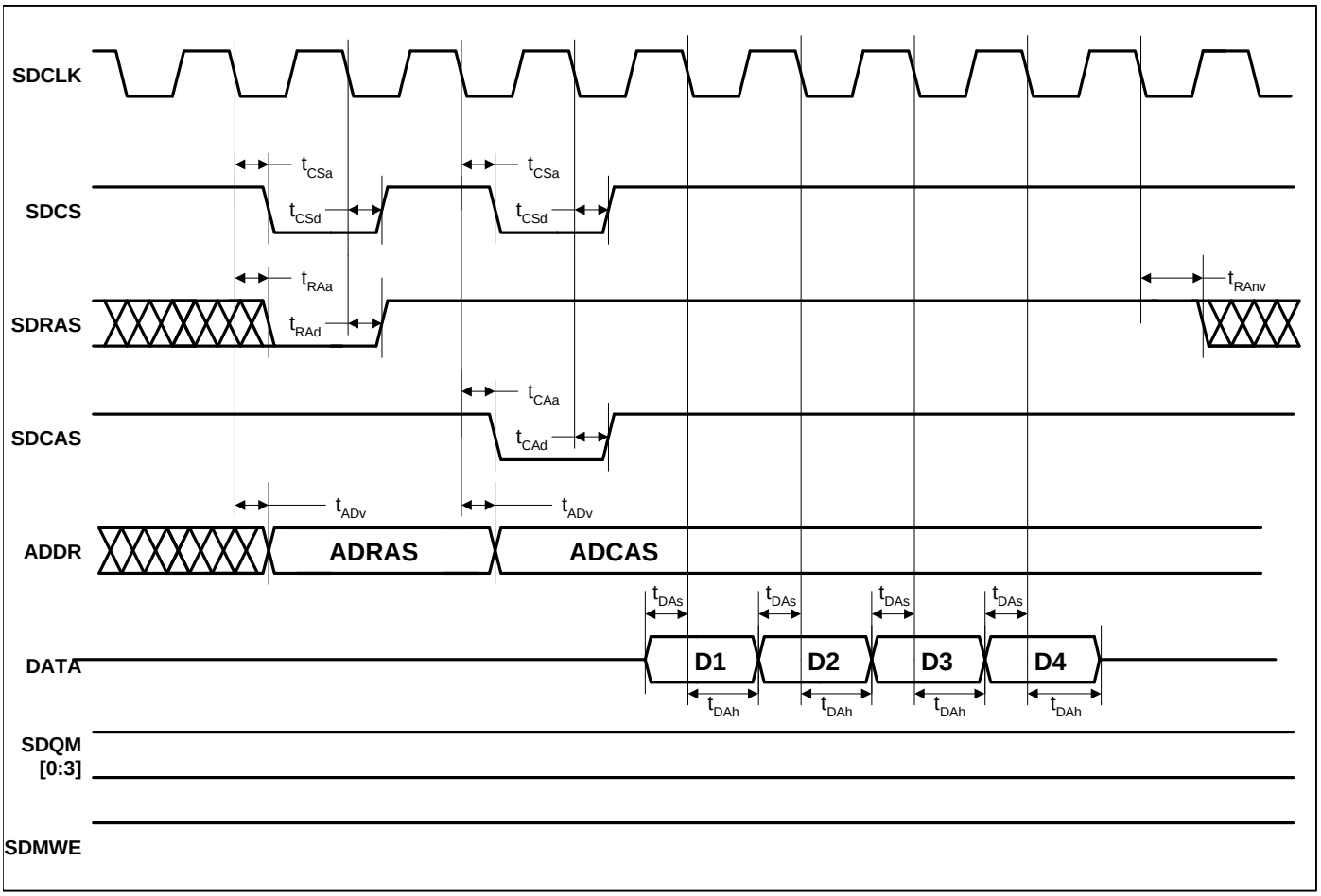


Figure 4. SDRAM Burst Read Cycle Timing Measurement

Note: 1. Timings are shown with CAS latency = 2
2. The SDCLK signal may be phase shifted relative to the rest of the SDRAM control and data signals due to uneven loading. Designers should take care to ensure that delays between SDRAM control and data signals are approximately equal.

SDRAM Burst Write Cycle

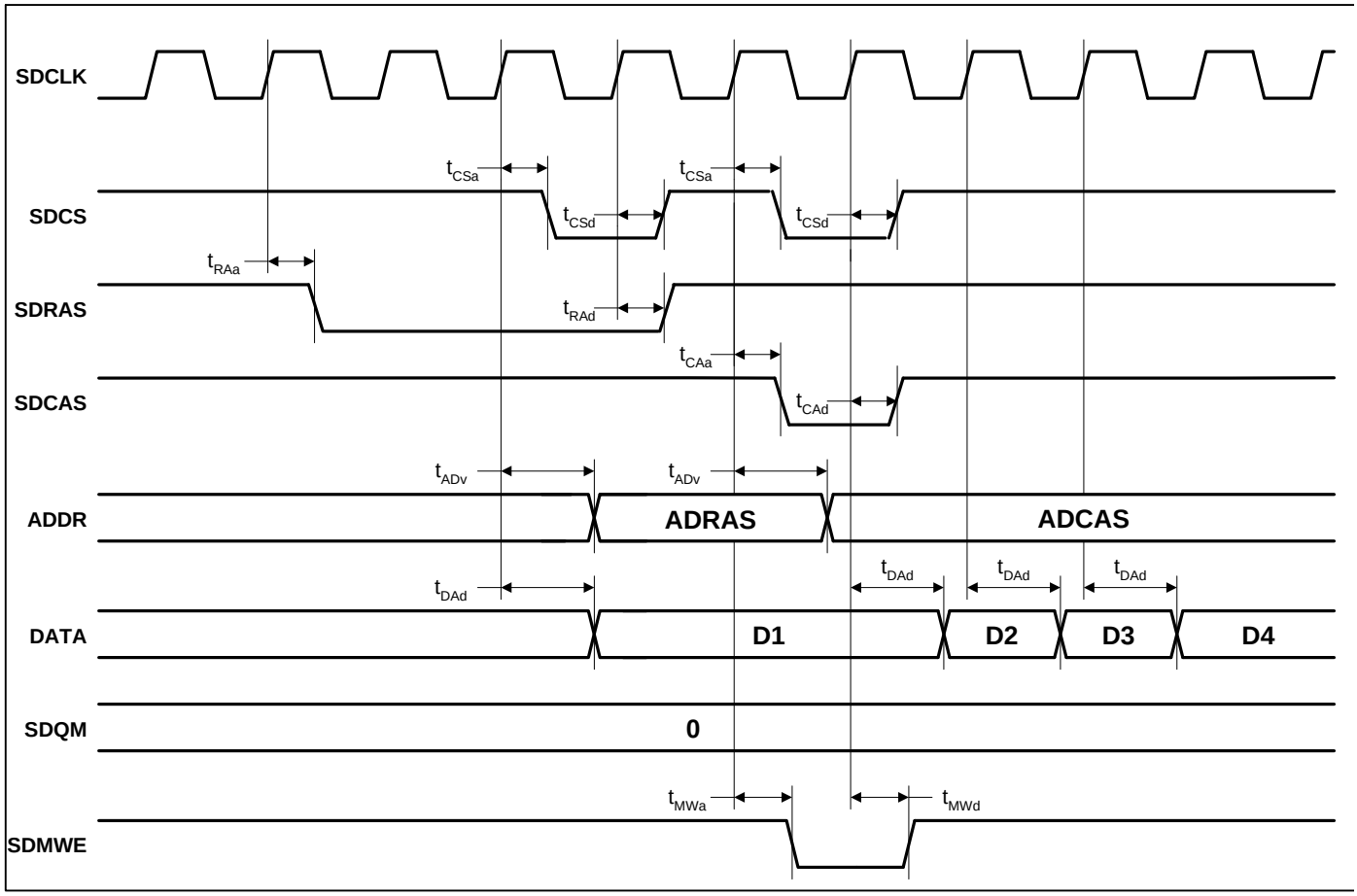


Figure 5. SDRAM Burst Write Cycle Timing Measurement

Note: 1. Timings are shown with CAS latency = 2
2. The SDCLK signal may be phase shifted relative to the rest of the SDRAM control and data signals due to uneven loading. Designers should take care to ensure that delays between SDRAM control and data signals are approximately equal

SDRAM Refresh Cycle

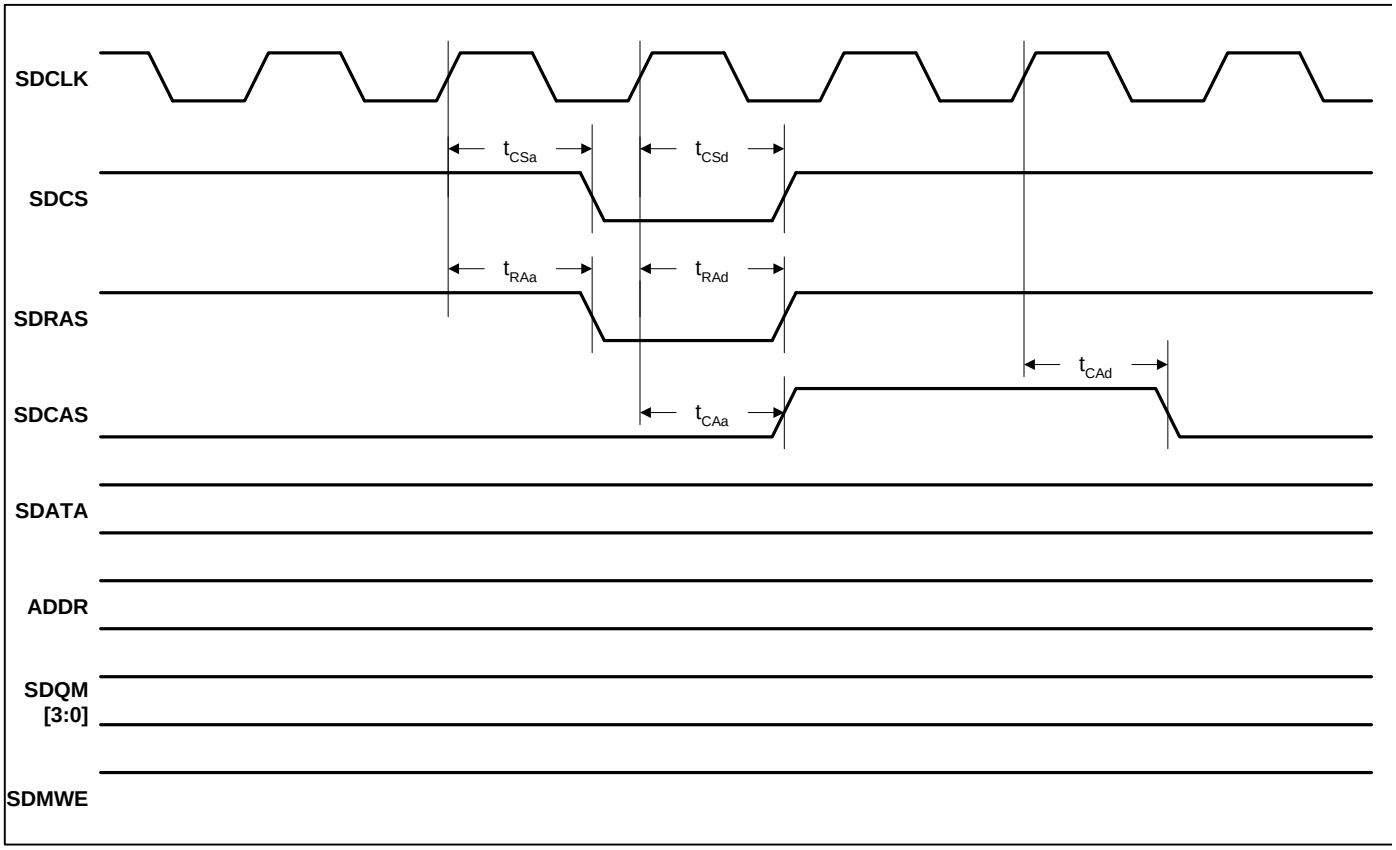


Figure 6. SDRAM Refresh Cycle Timing Measurement

Note: 1. Timings are shown with CAS latency = 2
2. The SDCLK signal may be phase shifted relative to the rest of the SDRAM control and data signals due to uneven loading. Designers should take care to ensure that delays between SDRAM control and data signals are approximately equal

Static Memory

Figure 7 through Figure 10 define the timings associated with all phases of the Static Memory. The following table contains the values for the timings of each of the Static Memory modes.

Parameter	Symbol	Min	Typ	Max	Unit
EXPCLK rising edge to nCS assert delay time	t_{CSd}	2	8	20	ns
EXPCLK falling edge to nCS deassert hold time	t_{CSh}	2	7	20	ns
EXPCLK rising edge to A assert delay time	t_{Ad}	4	9	16	ns
EXPCLK falling edge to A deassert hold time	t_{Ah}	3	10	19	ns
EXPCLK rising edge to nMWE assert delay time	t_{MWd}	3	6	10	ns
EXPCLK rising edge to nMWE deassert hold time	t_{MWh}	3	6	10	ns
EXPCLK falling edge to nMOE assert delay time	t_{MOEd}	3	7	10	ns
EXPCLK falling edge to nMOE deassert hold time	t_{MOEh}	2	7	10	ns
EXPCLK falling edge to HALFWORD deassert delay time	t_{HWd}	2	8	20	ns
EXPCLK falling edge to WORD assert delay time	t_{WDd}	2	8	16	ns
EXPCLK rising edge to data valid delay time	t_{Dv}	8	13	21	ns
EXPCLK falling edge to data invalid delay time	t_{Dnv}	6	15	30	ns
Data setup to EXPCLK falling edge time	t_{Ds}	-	-	1	ns
EXPCLK falling edge to data hold time	t_{Dh}	-	-	3	ns
EXPCLK rising edge to WRITE assert delay time	t_{WRd}	5	11	23	ns
EXPREADY setup to EXPCLK falling edge time	t_{EXs}	-	-	0	ns
EXPCLK falling edge to EXPREADY hold time	t_{EXh}	-	-	0	ns

Static Memory Single Read Cycle

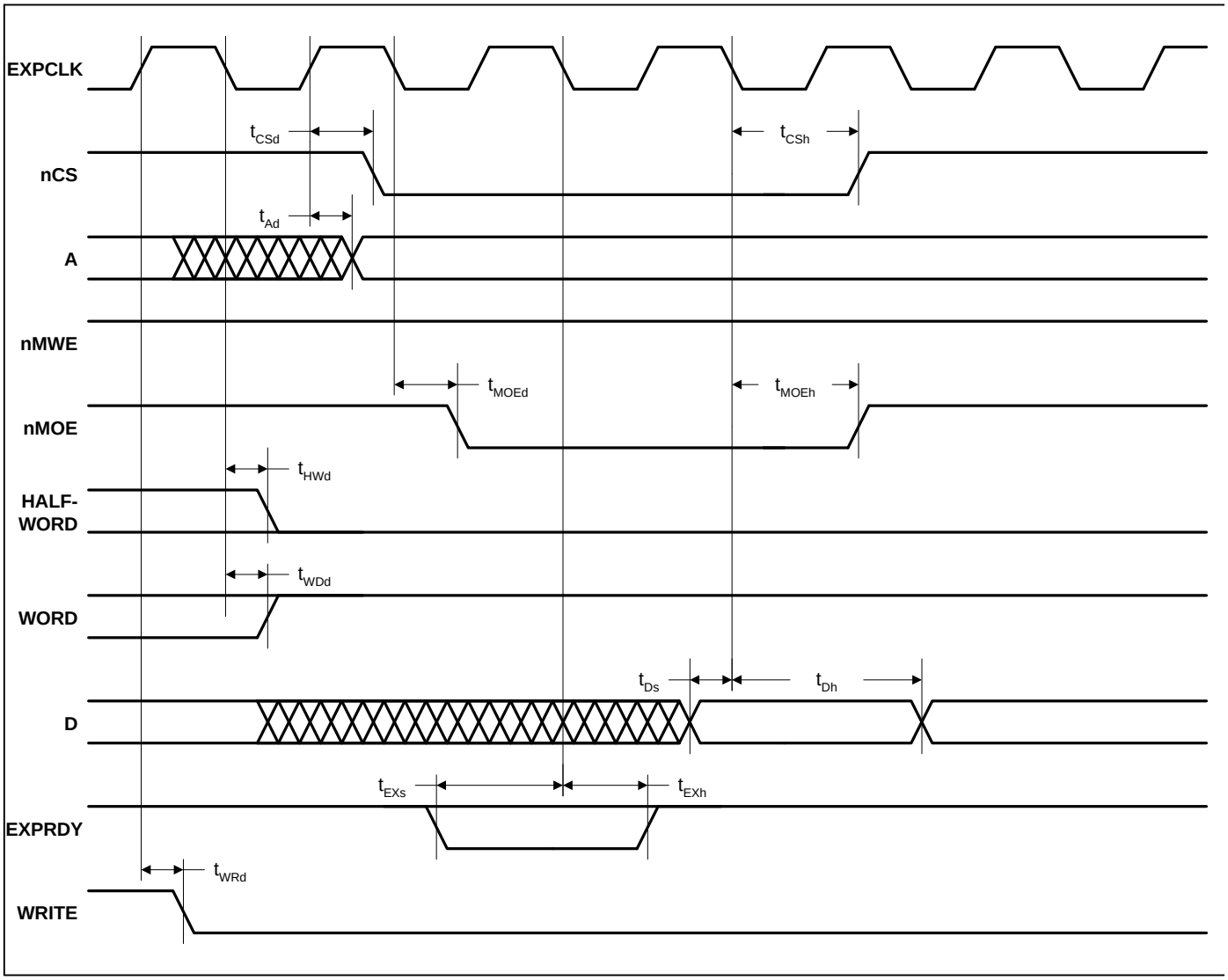


Figure 7. Static Memory Single Read Cycle Timing Measurement

Note: 1. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.
2. Address, Halfword, Word, and Write hold state until next cycle.

Static Memory Single Write Cycle

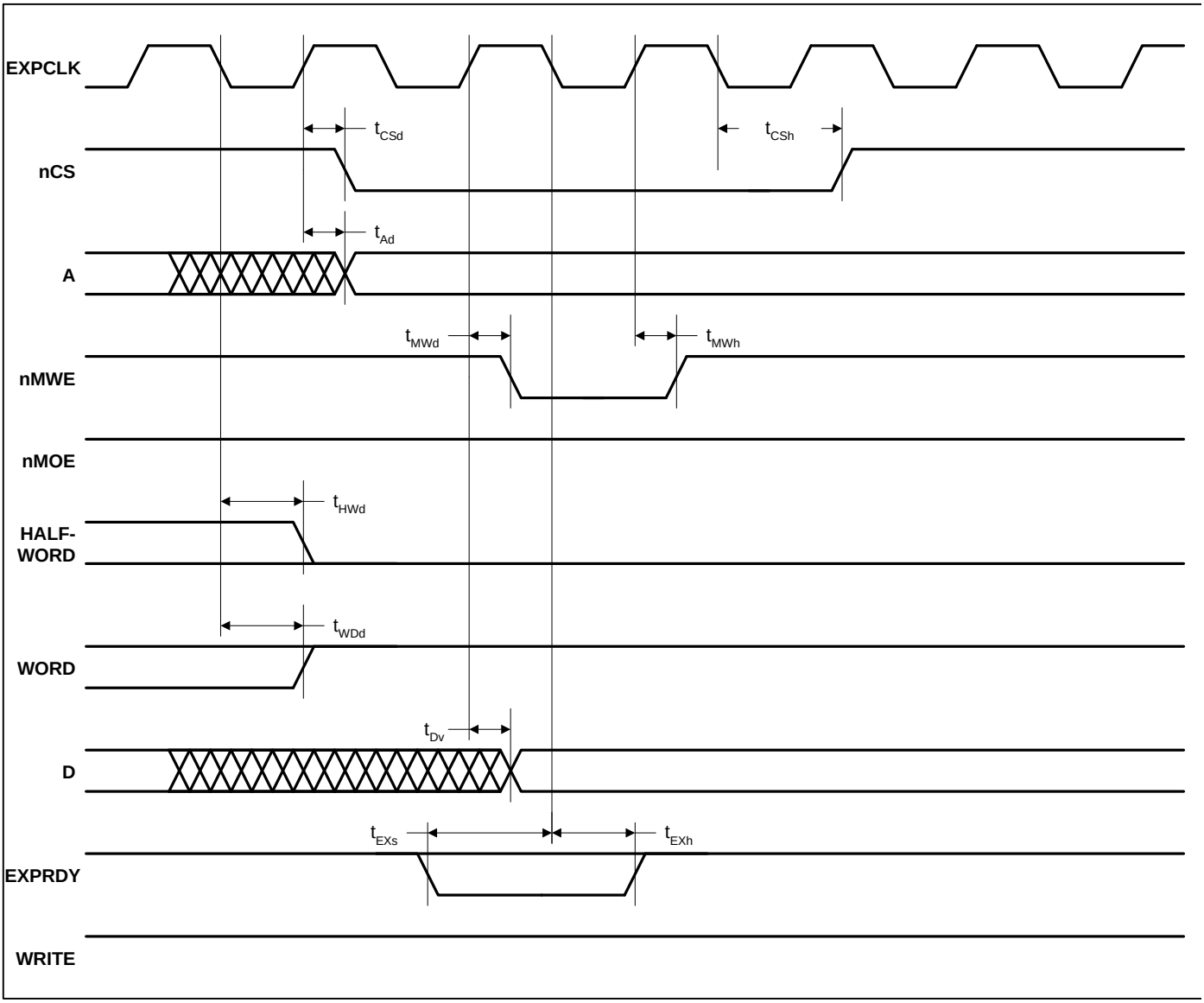


Figure 8. Static Memory Single Write Cycle Timing Measurement

Note: 1. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.

2. Zero wait states for sequential writes is not permitted for memory devices which use nMWE pin, as this cannot be driven with valid timing under zero wait state conditions.

3. Address, Data, Halfword, Word, and Write hold state until next cycle.

Static Memory Burst Read Cycle

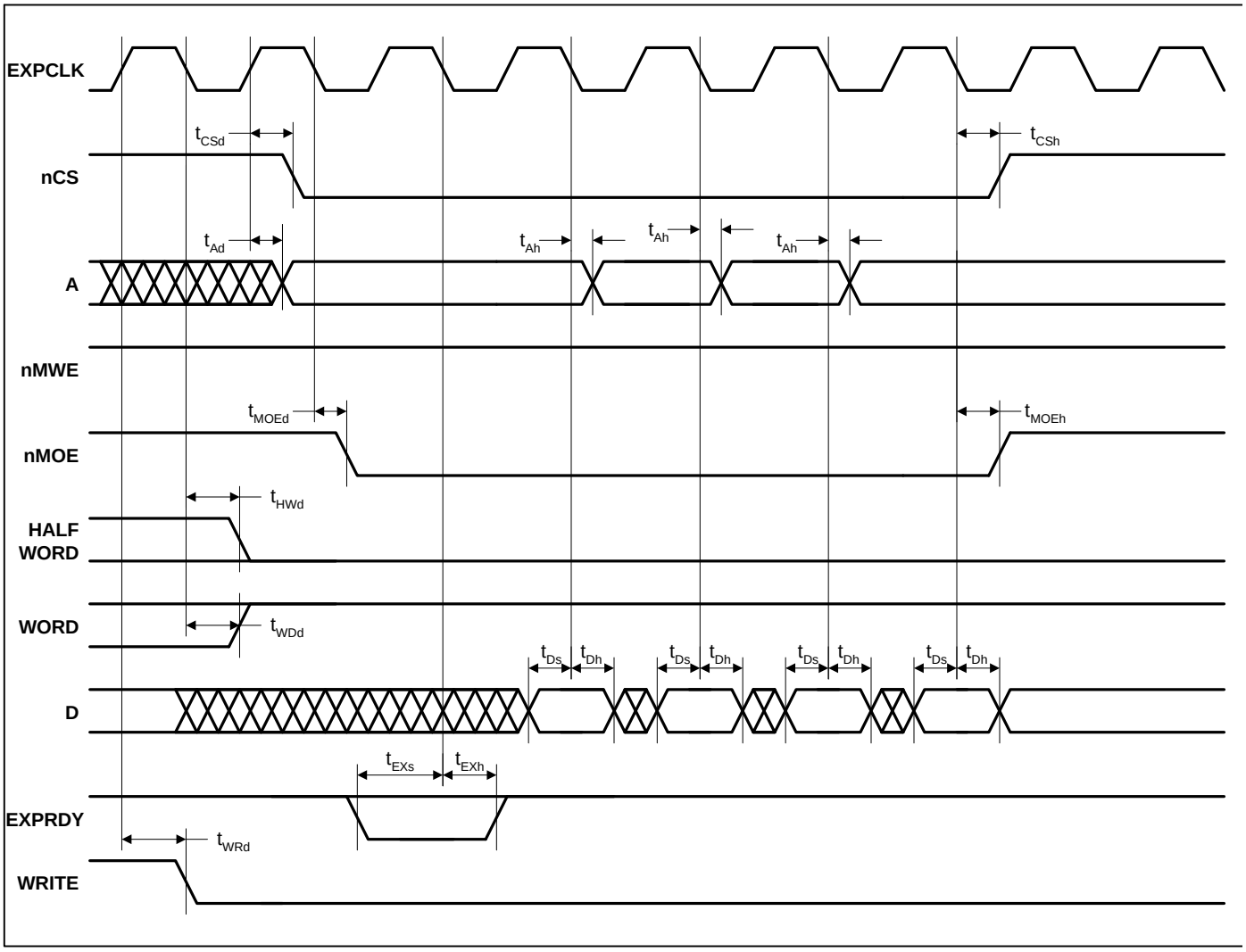


Figure 9. Static Memory Burst Read Cycle Timing Measurement

Note: 1. Four cycles are shown in the above diagram (minimum wait states, 1-0-0-0). This is the maximum number of consecutive cycles that can be driven. The number of consecutive cycles can be programmed from 2 to 4, inclusively.
2. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.
3. Consecutive reads with sequential access enabled are identical except that the sequential access wait state field is used to determine the number of wait states, and no idle cycles are inserted between successive non-sequential ROM/expansion cycles. This improves performance so the SQAEN bit should always be set where possible.
4. Address, Halfword, Word, and Write hold state until next cycle.

Static Memory Burst Write Cycle

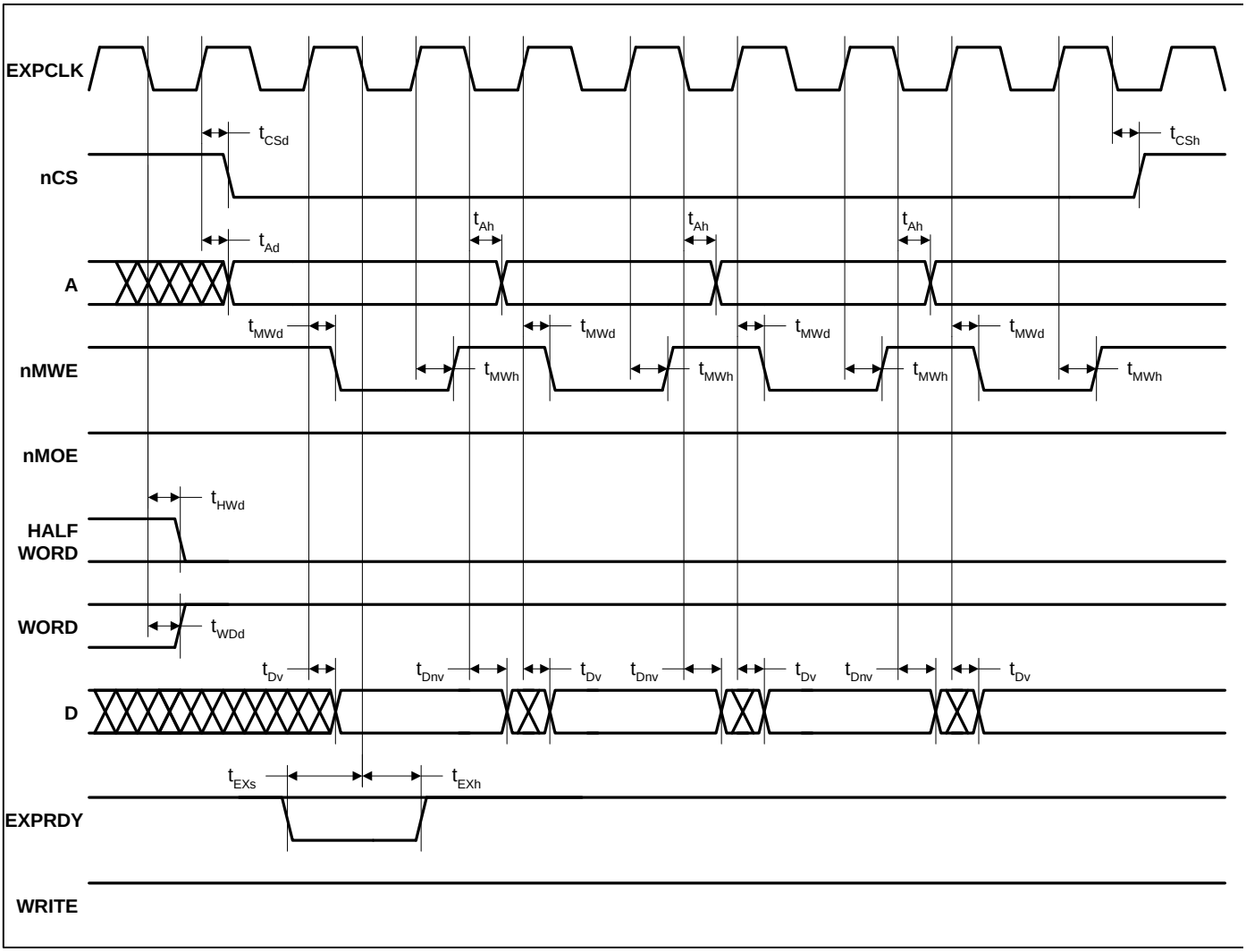


Figure 10. Static Memory Burst Write Cycle Timing Measurement

Note: 1. Four cycles are shown in the above diagram (minimum wait states, 1-1-1-1). This is the maximum number of consecutive cycles that can be driven. The number of consecutive cycles can be programmed from 2 to 4, inclusively.
2. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.
3. Zero wait states for sequential writes is not permitted for memory devices which use nMWE pin, as this cannot be driven with valid timing under zero wait state conditions.
4. Address, Data, Halfword, Word, and Write hold state until next cycle.

SSI1 Interface

Parameter	Symbol	Min	Max	Unit
ADCCLK falling edge to nADCCSS deassert delay time	t_{Cd}	9	10	ms
ADCIN data setup to ADCCLK rising edge time	t_{INs}	-	15	ns
ADCIN data hold from ADCCLK rising edge time	t_{INh}	-	14	ns
ADCCLK falling edge to data valid delay time	t_{Ovd}	– 7	13	ns
ADCCLK falling edge to data invalid delay time	t_{Od}	– 2	3	ns

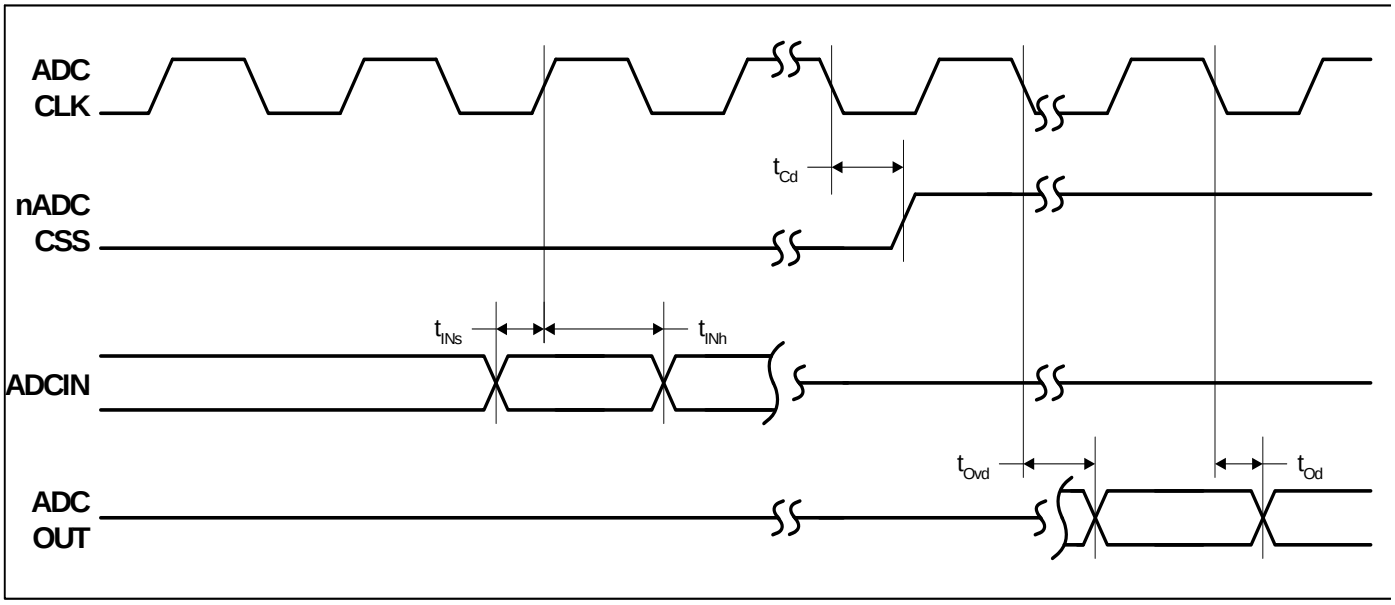


Figure 11. SSI1 Interface Timing Measurement

SSI2 Interface

Parameter	Symbol	Min	Max	Unit
SSICLK period (slave mode)	t_{clk_per}	185	2050	ns
SSICLK high time	t_{clk_high}	925	1025	ns
SSICLK low time	t_{clk_low}	925	1025	ns
SSICLK rise/fall time	t_{clkrf}	3	18	ns
SSICLK rising edge to RX and/or TX frame sync high time	t_{FRd}	-	3	ns
SSICLK rising edge to RX and/or TX frame sync low time	t_{FRa}	-	8	ns
SSIRXFR and/or SSITXFR period	t_{FR_per}	960	990	ns
SSIRXDA setup to SSICLK falling edge time	t_{RXs}	3	7	ns
SSIRXDA hold from SSICLK falling edge time	t_{RXh}	3	7	ns
SSICLK rising edge to SSITXDA data valid delay time	t_{TXd}	-	2	ns
SSITXDA valid time	t_{TXv}	960	990	ns

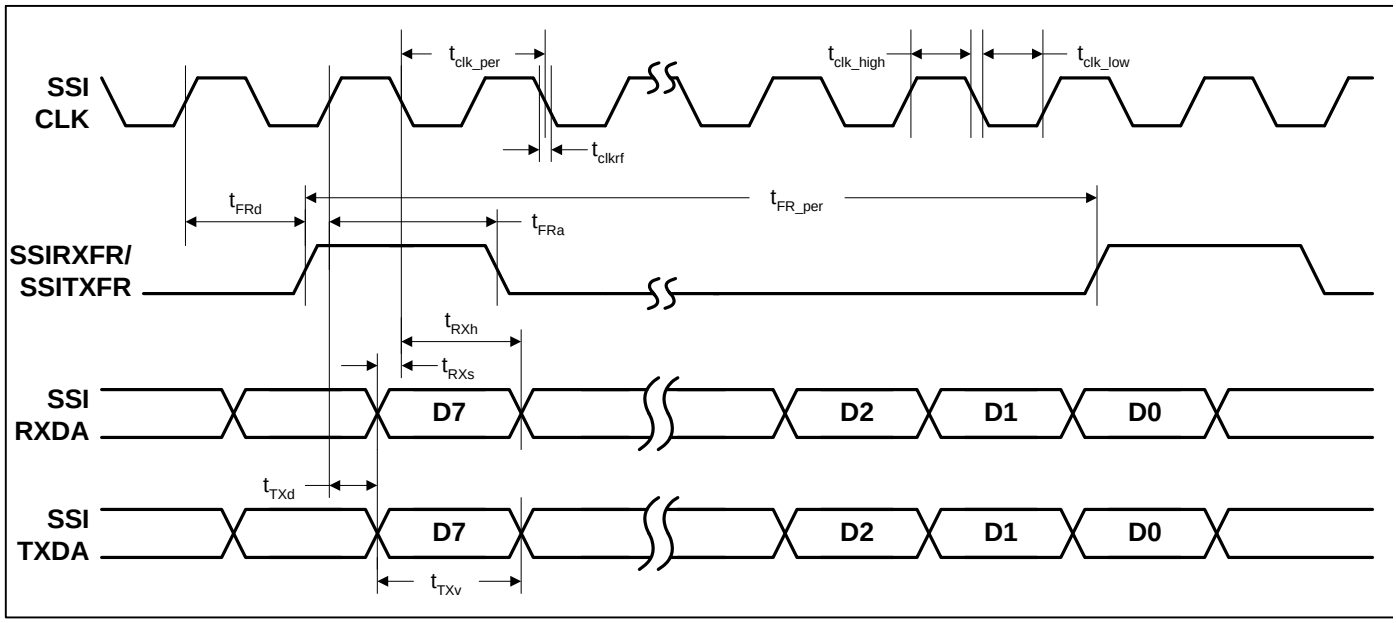


Figure 12. SSI2 Interface Timing Measurement

LCD Interface

Parameter	Symbol	Min	Max	Unit
CL[2] falling to CL[1] rising delay time	t_{CL1d}	– 10	25	ns
CL[1] falling to CL[2] rising delay time	t_{CL2d}	80	3,475	ns
CL[1] falling to FRM transition time	t_{FRMd}	300	10,425	ns
CL[1] falling to M transition time	t_{Md}	– 10	20	ns
CL[2] rising to DD (display data) transition time	t_{DDd}	– 10	20	ns

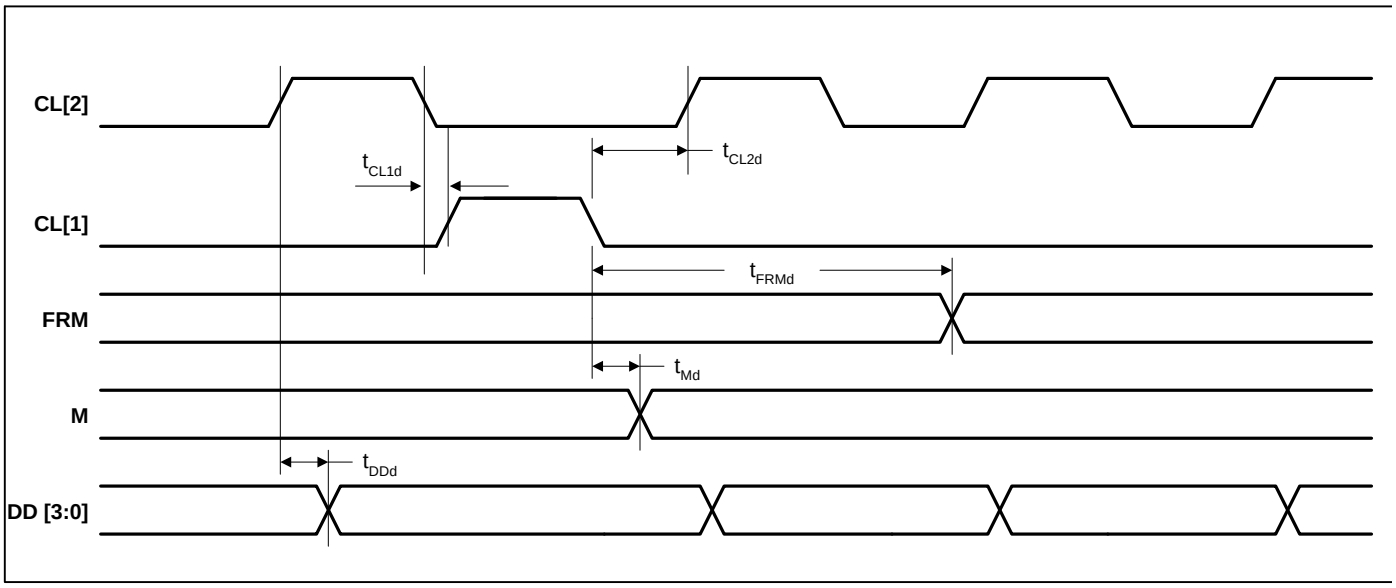


Figure 13. LCD Controller Timing Measurement

JTAG Interface

Parameter	Symbol	Min	Max	Units
TCK clock period	t_{clk_per}	2	-	ns
TCK clock high time	t_{clk_high}	1	-	ns
TCK clock low time	t_{clk_low}	1	-	ns
JTAG port setup time	t_{JPs}	-	0	ns
JTAG port hold time	t_{JPh}	-	3	ns
JTAG port clock to output	t_{JPco}	-	10	ns
JTAG port high impedance to valid output	t_{JPzx}	-	12	ns
JTAG port valid output to high impedance	t_{JPxz}	-	19	ns

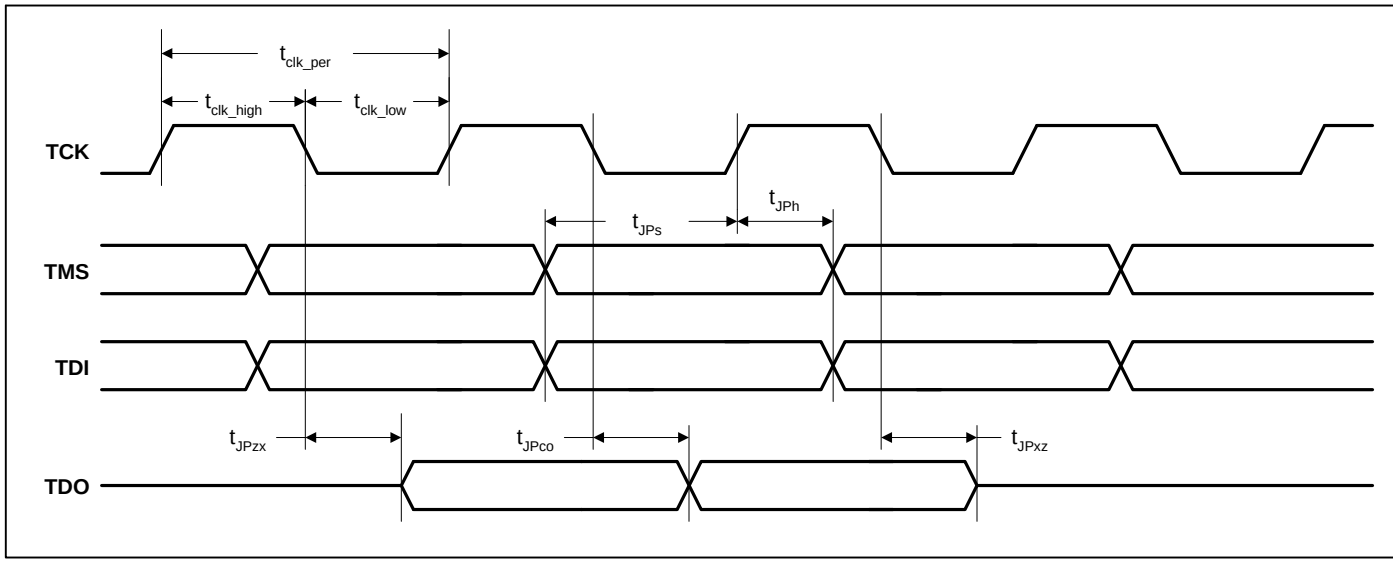
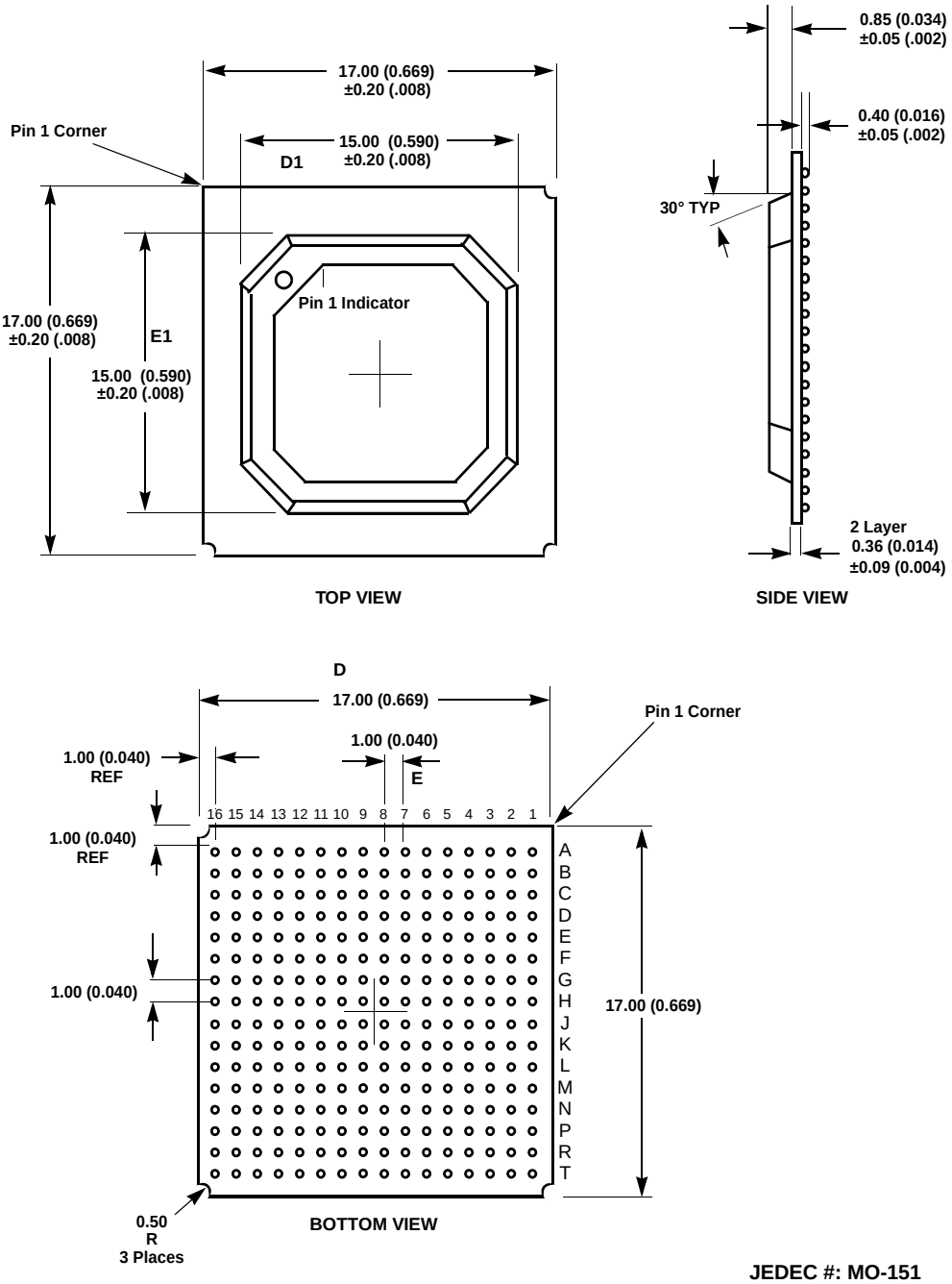


Figure 14. JTAG Timing Measurement

Packages

256-Ball PBGA Package Characteristics

256-Ball PBGA Package Specifications



JEDEC #: MO-151
Ball Diameter: 0.50 mm ± 0.10 mm
17 ¥ 17 ¥ 1.61 mm body

Figure 15. 256-Ball PBGA Package

Note: 1) For pin locations see Table T.
2) Dimensions are in millimeters (inches), and controlling dimension is millimeter
3) Before beginning any new EP7311 design, contact Cirrus Logic for the latest package information.

256-Ball PBGA Pinout (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VDDIO	nCS[4]	nCS[1]	SDCLK	SDQM[3]	DD[1]	M	VDDIO	D[0]	D[2]	A[3]	VDDIO	A[6]	MOSCOUT	VDDOSC	VSSIO	A
B	nCS[5]	VDDIO	nCS[3]	nMOE/ nSDCAS	VDDIO	nSDCS[1]	DD[2]	CL[1]	VDDCORE	D[1]	A[2]	A[4]	A[5]	WAKEUP	VDDIO	nURESET	B
C	VDDIO	EXPCLK	VSSIO	VDDIO	VSSIO	VSSIO	VSSIO	VDDIO	VSSIO	VSSIO	VSSIO	VDDIO	VSSIO	VSSIO	nPOR	nEXTPWR	C
D	WRITE/ nSDRAS	EXPRDY	VSSIO	VDDIO	nCS[2]	nMWE/ nSDWE	nSDCS[0]	CL[2]	VSSRTC	D[4]	nPWRFL	MOSCIN	VDDIO	VSSIO	D[7]	D[8]	D
E	RXD[2]	PB[7]	TDI	WORD	VSSIO	nCS[0]	SDQM[2]	FRM	A[0]	D[5]	VSSOSC	VSSIO	nMEDCHG/ nBROM	VDDIO	D[9]	D[10]	E
F	PB[5]	PB[3]	VSSIO	TXD[2]	RUN/ CLKEN	VSSIO	SDCKE	DD[3]	A[1]	D[6]	VSSRTC	BATOK	nBATCHG	VSSIO	D[11]	VDDIO	F
G	PB[1]	VDDIO	TDO	PB[4]	PB[6]	VSSRTC	VSSRTC	DD[0]	D[3]	VSSRTC	A[7]	A[8]	A[9]	VSSIO	D[12]	D[13]	G
H	PA[7]	PA[5]	VSSIO	PA[4]	PA[6]	PB[0]	PB[2]	VSSRTC	VSSRTC	A[10]	A[11]	A[12]	A[13]/ DRA[14]	VSSIO	D[14]	D[15]	H
J	PA[3]	PA[1]	VSSIO	PA[2]	PA[0]	TXD[1]	CTS	VSSRTC	VSSRTC	A[17]/ DRA[10]	A[16]/ DRA[11]	A[15]/ DRA[12]	A[14]/ DRA[13]	nTRST	D[16]	D[17]	J
K	LEDDRV	PHDIN	VSSIO	DCD	nTEST[1]	EINT[3]	VSSRTC	ADCIN	COL[4]	TCLK	D[20]	D[19]	D[18]	VSSIO	VDDIO	VDDIO	K
L	RXD[1]	DSR	VDDIO	nEINT[1]	PE[2]/ CLKSEL	VSSRTC	PD[0]/ LEDFLSH	VSSRTC	COL[6]	D[31]	VSSRTC	A[22]/ DRA[5]	A[21]/ DRA[6]	VSSIO	A[18]/ DRA[9]	A[19]/ DRA[8]	L
M	nTEST[0]	nEINT[2]	VDDIO	PE[0]/ BOOTSEL[0]	TMS	VDDIO	SSITXFR	DRIVE[1]	FB[0]	COL[0]	D[27]	VSSIO	A[23]/ DRA[4]	VDDIO	A[20]/ DRA[7]	D[21]	M
N	nEXTFIQ	PE[1]/ BOOTSEL[1]	VSSIO	VDDIO	PD[5]	PD[2]	SSIRXDA	ADCCLK	SMPCLK	COL[2]	D[29]	D[26]	HALFWORD	VSSIO	D[22]	D[23]	N
P	VSSRTC	RTCOUT	VSSIO	VSSIO	VDDIO	VSSIO	VSSIO	VDDIO	VSSIO	VDDIO	VSSIO	VSSIO	VDDIO	VSSIO	D[24]	VDDIO	P
R	RTCIN	VDDIO	PD[4]	PD[1]	SSITXDA	nADCCS	VDDIO	ADCOUT	COL[7]	COL[3]	COL[1]	D[30]	A[27]/ DRA[0]	A[25]/ DRA[2]	VDDIO	A[24]\ DRA[3]	R
T	VDDRTC	PD[7]/ SDQM[1]	PD[6]/ SDQM[0]	PD[3]	SSICLK	SSIRXFR	VDDCORE	DRIVE[0]	FB[1]	COL[5]	VDDIO	BUZ	D[28]	A[26]/ DRA[1]	D[25]	VSSIO	T

256-Ball PBGA Ball Listing

The list is ordered by ball location.

Table T. 256-Ball PBGA Ball Listing

Ball Location	Name	Type	Description
A1	VDDIO	Pad power	Digital I/O power, 3.3V
A2	nCS[4]	O	Chip select out
A3	nCS[1]	O	Chip select out
A4	SDCLK	O	SDRAM clock out
A5	SDQM[3]	O	SDRAM byte lane mask
A6	DD[1]	O	LCD serial display data
A7	M	O	LCD AC bias drive
A8	VDDIO	Pad power	Digital I/O power, 3.3V
A9	D[0]	I/O	Data I/O
A10	D[2]	I/O	Data I/O
A11	A[3]	O	System byte address
A12	VDDIO	Pad power	Digital I/O power, 3.3V
A13	A[6]	O	System byte address
A14	MOSCOUT	O	Main oscillator out
A15	VDDOSC	Oscillator power	Oscillator power in, 2.5V
A16	VSSIO	Pad ground	I/O ground
B1	nCS[5]	O	Chip select out
B2	VDDIO	Pad power	I/O ground
B3	nCS[3]	O	Chip select out
B4	nMOE/nSDCAS	O	ROM, expansion OP enable/SDRAM CAS control signal
B5	VDDIO	Pad power	Digital I/O power, 3.3V
B6	nSDCS[1]	O	SDRAM chip select out
B7	DD[2]	O	LCD serial display data
B8	CL[1]	O	LCD line clock
B9	VDDCORE	Core power	Digital core power, 2.5V
B10	D[1]	I/O	Data I/O
B11	A[2]	O	System byte address
B12	A[4]	O	System byte address
B13	A[5]	O	System byte address
B14	WAKEUP	I	System wake up input
B15	VDDIO	Pad power	Digital I/O power, 3.3V
B16	nURESET	I	User reset input
C1	VDDIO	Pad power	Digital I/O power, 3.3V
C2	EXPCLK	I	Expansion clock input
C3	VSSIO	Pad ground	I/O ground
C4	VDDIO	Pad power	Digital I/O power, 3.3V
C5	VSSIO	Pad ground	I/O ground
C6	VSSIO	Pad ground	I/O ground
C7	VSSIO	Pad ground	I/O ground
C8	VDDIO	Pad power	Digital I/O power, 3.3V
C9	VSSIO	Pad ground	I/O ground
C10	VSSIO	Pad ground	I/O ground
C11	VSSIO	Pad ground	I/O ground

Table T. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Type	Description
C12	VDDIO	Pad power	Digital I/O power, 3.3V
C13	VSSIO	Pad ground	I/O ground
C14	VSSIO	Pad ground	I/O ground
C15	nPOR	I	Power-on reset input
C16	nEXTPWR	I	External power supply sense input
D1	WRITE/nSDRAS	O	Transfer direction / SDRAM RAS signal output
D2	EXPRDY	I	Expansion port ready input
D3	VSSIO	Pad ground	I/O ground
D4	VDDIO	Pad power	Digital I/O power, 3.3V
D5	nCS[2]	O	Chip select out
D6	nMWE/nSDWE	O	ROM, expansion write enable/ SDRAM write enable control signal
D7	nSDCS[0]	O	SDRAM chip select out
D8	CL[2]	O	LCD pixel clock out
D9	VSSRTC	Core ground	Real time clock ground
D10	D[4]	I/O	Data I/O
D11	nPWRFL	I	Power fail sense input
D12	MOSCIN	I	Main oscillator input
D13	VDDIO	Pad power	Digital I/O power, 3.3V
D14	VSSIO	Pad ground	I/O ground
D15	D[7]	I/O	Data I/O
D16	D[8]	I/O	Data I/O
E1	RXD[2]	I	UART 2 receive data input
E2	PB[7]	I	GPIO port B
E3	TDI	I	JTAG data input
E4	WORD	O	Word access select output
E5	VSSIO	Pad ground	I/O ground
E6	nCS[0]	O	Chip select out
E7	SDQM[2]	O	SDRAM byte lane mask
E8	FRM	O	LCD frame synchronization pulse
E9	A[0]	O	System byte address
E10	D[5]	I/O	Data I/O
E11	VSSOSC	Oscillator ground	PLL ground
E12	VSSIO	Pad ground	I/O ground
E13	nMEDCHG/nBROM	I	Media change interrupt input / internal ROM boot enable
E14	VDDIO	Pad power	Digital I/O power, 3.3V
E15	D[9]	I/O	Data I/O
E16	D[10]	I/O	Data I/O
F1	PB[5]	I	GPIO port B
F2	PB[3]	I	GPIO port B
F3	VSSIO	Pad ground	I/O ground
F4	TXD[2]	O	UART 2 transmit data output
F5	RUN/CLKEN	O	Run output / clock enable output
F6	VSSIO	Pad ground	I/O ground

Table T. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Type	Description
F7	SDCKE	O	SDRAM clock enable output
F8	DD[3]	O	LCD serial display data
F9	A[1]	O	System byte address
F10	D[6]	I/O	Data I/O
F11	VSSRTC	RTC ground	Real time clock ground
F12	BATOK	I	Battery ok input
F13	nBATCHG	I	Battery changed sense input
F14	VSSIO	Pad ground	I/O ground
F15	D[11]	I/O	Data I/O
F16	VDDIO	Pad power	Digital I/O power, 3.3V
G1	PB[1]	I	GPIO port B
G2	VDDIO	Pad power	Digital I/O power, 3.3V
G3	TDO	O	JTAG data out
G4	PB[4]	I	GPIO port B
G5	PB[6]	I	GPIO port B
G6	VSSRTC	Core ground	Real time clock ground
G7	VSSRTC	RTC ground	Real time clock ground
G8	DD[0]	O	LCD serial display data
G9	D[3]	I/O	Data I/O
G10	VSSRTC	RTC ground	Real time clock ground
G11	A[7]	O	System byte address
G12	A[8]	O	System byte address
G13	A[9]	O	System byte address
G14	VSSIO	Pad ground	I/O ground
G15	D[12]	I/O	Data I/O
G16	D[13]	I/O	Data I/O
H1	PA[7]	I	GPIO port A
H2	PA[5]	I	GPIO port A
H3	VSSIO	Pad ground	I/O ground
H4	PA[4]	I	GPIO port A
H5	PA[6]	I	GPIO port A
H6	PB[0]	I	GPIO port B
H7	PB[2]	I	GPIO port B
H8	VSSRTC	RTC ground	Real time clock ground
H9	VSSRTC	RTC ground	Real time clock ground
H10	A[10]	O	System byte address
H11	A[11]	O	System byte address
H12	A[12]	O	System byte address
H13	A[13]/DRA[14]	O	System byte address / SDRAM address
H14	VSSIO	Pad ground	I/O ground
H15	D[14]	I/O	Data I/O
H16	D[15]	I/O	Data I/O
J1	PA[3]	I	GPIO port A
J2	PA[1]	I	GPIO port A
J3	VSSIO	Pad ground	I/O ground
J4	PA[2]	I	GPIO port A
J5	PA[0]	I	GPIO port A
J6	TXD[1]	O	UART 1 transmit data out

Table T. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Type	Description
J7	CTS	I	UART 1 clear to send input
J8	VSSRTC	RTC ground	Real time clock ground
J9	VSSRTC	RTC ground	Real time clock ground
J10	A[17]/DRA[10]	O	System byte address / SDRAM address
J11	A[16]/DRA[11]	O	System byte address / SDRAM address
J12	A[15]/DRA[12]	O	System byte address / SDRAM address
J13	A[14]/DRA[13]	O	System byte address / SDRAM address
J14	nTRST	I	JTAG async reset input
J15	D[16]	I/O	Data I/O
J16	D[17]	I/O	Data I/O
K1	LEDDRV	O	IR LED drivet
K2	PHDIN	I	Photodiode input
K3	VSSIO	Pad ground	I/O ground
K4	DCD	I	UART 1 data carrier detect
K5	nTEST[1]	I	Test mode select input
K6	EINT[3]	I	External interrupt
K7	VSSRTC	RTC ground	Real time clock ground
K8	ADCIN	I	SSI1 ADC serial input
K9	COL[4]	O	Keyboard scanner column drive
K10	TCLK	I	JTAG clock
K11	D[20]	I/O	Data I/O
K12	D[19]	I/O	Data I/O
K13	D[18]	I/O	Data I/O
K14	VSSIO	Pad ground	I/O ground
K15	VDDIO	Pad power	Digital I/O power, 3.3V
K16	VDDIO	Pad power	Digital I/O power, 3.3V
L1	RXD[1]	I	UART 1 receive data input
L2	DSR	I	UART 1 data set ready input
L3	VDDIO	Pad power	Digital I/O power, 3.3V
L4	nEINT[1]	I	External interrupt input
L5	PE[2]/CLKSEL	I	GPIO port E / clock input mode select
L6	VSSRTC	RTC ground	Real time clock ground
L7	PD[0]/LEDFLSH	I/O	GPIO port D / LED blinker output
L8	VSSRTC	Core ground	Real time clock ground
L9	COL[6]	O	Keyboard scanner column drive
L10	D[31]	I/O	Data I/O
L11	VSSRTC	RTC ground	Real time clock ground
L12	A[22]/DRA[5]	O	System byte address / SDRAM address
L13	A[21]/DRA[6]	O	System byte address / SDRAM address
L14	VSSIO	Pad ground	I/O ground
L15	A[18]/DRA[9]	O	System byte address / SDRAM address
L16	A[19]/DRA[8]	O	System byte address / SDRAM address
M1	nTEST[0]	I	Test mode select input
M2	nEINT[2]	I	External interrupt input
M3	VDDIO	Pad power	Digital I/O power, 3.3V
M4	PE[0]/BOOTSEL[0]	I	GPIO port E / Boot mode select
M5	TMS	I	JTAG mode select
M6	VDDIO	Pad power	Digital I/O power, 3.3V

Table T. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Type	Description
M7	SSITXFR	I/O	MCP/CODEC/SSI2 frame sync
M8	DRIVE[1]	I/O	PWM drive output
M9	FB[0]	I	PWM feedback input
M10	COL[0]	O	Keyboard scanner column drive
M11	D[27]	I/O	Data I/O
M12	VSSIO	Pad ground	I/O ground
M13	A[23]/DRA[4]	O	System byte address / SDRAM address
M14	VDDIO	Pad power	Digital I/O power, 3.3V
M15	A[20]/DRA[7]	O	System byte address / SDRAM address
M16	D[21]	I/O	Data I/O
N1	nEXTFIQ	I	External fast interrupt input
N2	PE[1]/BOOTSEL[1]	I	GPIO port E / boot mode select
N3	VSSIO	Pad ground	I/O ground
N4	VDDIO	Pad power	Digital I/O power, 3.3V
N5	PD[5]	I/O	GPIO port D
N6	PD[2]	I/O	GPIO port D
N7	SSIRXDA	I/O	MCP/CODEC/SSI2 serial data input
N8	ADCCLK	O	SSI1 ADC serial clock
N9	SMPCLK	O	SSI1 ADC sample clock
N10	COL[2]	O	Keyboard scanner column drive
N11	D[29]	I/O	Data I/O
N12	D[26]	I/O	Data I/O
N13	HALFWORD	O	Halfword access select output
N14	VSSIO	Pad ground	I/O ground
N15	D[22]	I/O	Data I/O
N16	D[23]	I/O	Data I/O
P1	VSSRTC	RTC ground	Real time clock ground
P2	RTCOUT	O	Real time clock oscillator output
P3	VSSIO	Pad ground	I/O ground
P4	VSSIO	Pad ground	I/O ground
P5	VDDIO	Pad power	Digital I/O power, 3.3V
P6	VSSIO	Pad ground	I/O ground
P7	VSSIO	Pad ground	I/O ground
P8	VDDIO	Pad power	Digital I/O power, 3.3V
P9	VSSIO	Pad ground	I/O ground
P10	VDDIO	Pad power	Digital I/O power, 3.3V
P11	VSSIO	Pad ground	I/O ground
P12	VSSIO	Pad ground	I/O ground
P13	VDDIO	Pad power	Digital I/O power
P14	VSSIO	Pad ground	I/O ground
P15	D[24]	I/O	Data I/O
P16	VDDIO	Pad power	Digital I/O power, 3.3V
R1	RTCIN	I/O	Real time clock oscillator input
R2	VDDIO	Pad power	Digital I/O power, 3.3V
R3	PD[4]	I/O	GPIO port D
R4	PD[1]	I/O	GPIO port D
R5	SSITXDA	O	MCP/CODEC/SSI2 serial data output
R6	nADCCS	O	SSI1 ADC chip select

Table T. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Type	Description
R7	VDDIO	Pad power	Digital I/O power, 3.3V
R8	ADCOUT	O	SSI1 ADC serial data output
R9	COL[7]	O	Keyboard scanner column drive
R10	COL[3]	O	Keyboard scanner column drive
R11	COL[1]	O	Keyboard scanner column drive
R12	D[30]	I/O	Data I/O
R13	A[27]/DRA[0]	O	System byte address / SDRAM address
R14	A[25]/DRA[2]	O	System byte address / SDRAM address
R15	VDDIO	Pad power	Digital I/O power, 3.3V
R16	A[24]/DRA[3]	O	System byte address / SDRAM address
T1	VDDRTC	RTC power	Real time clock power, 2.5V
T2	PD[7]/SDQM[1]	I/O	GPIO port D / SDRAM byte lane mask
T3	PD[6]/SDQM[0]	I/O	GPIO port D / SDRAM byte lane mask
T4	PD[3]	I/O	GPIO port D
T5	SSICLK	I/O	MCP/CODEC/SSI2 serial clock
T6	SSIRXFR	–	MCP/CODEC/SSI2 frame sync
T7	VDDCORE	Core power	Core power, 2.5V
T8	DRIVE[0]	I/O	PWM drive output
T9	FB[1]	I	PWM feedback input
T10	COL[5]	O	Keyboard scanner column drive
T11	VDDIO	Pad power	Digital I/O power, 3.3V
T12	BUZ	O	Buzzer drive output
T13	D[28]	I/O	Data I/O
T14	A[26]/DRA[1]	O	System byte address / SDRAM address
T15	D[25]	I/O	Data I/O
T16	VSSIO	Pad ground	I/O ground

JTAG Boundary Scan Signal Ordering

Table U. JTAG Boundary Scan Signal Ordering

PBGA Ball	Signal	Type	Position
B1	nCS[5]	O	1
C2	EXPCLK	I/O	3
E4	WORD	O	6
D1	WRITE/nSDRAS	O	8
F5	RUN/CLKEN	O	10
D2	EXPRDY	I	13
F4	TXD2	O	14
E1	RXD2	I	16
E2	PB[7]	I/O	17
G5	PB[6]	I/O	20
F1	PB[5]	I/O	23
G4	PB[4]	I/O	26
F2	PB[3]	I/O	29
H7	PB[2]	I/O	32
G1	PB[1]/PRDY2	I/O	35
H6	PB[0]/PRDY1	I/O	38
H1	PA[7]	I/O	41
H5	PA[6]	I/O	44
H2	PA[5]	I/O	47
H4	PA[4]	I/O	50
J1	PA[3]	I/O	53
J4	PA[2]	I/O	56
J2	PA[1]	I/O	59
J5	PA[0]	I/O	62
K1	LEDDRV	O	65
J6	TXD1	O	67
K2	PHDIN	I	69
J7	CTS	I	70
L1	RXD1	I	71
K4	DCD	I	72
L2	DSR	I	73
K5	nTEST1	I	74
M1	nTEST0	I	75
K6	EINT3	I	76
M2	nEINT2	I	77
L4	nEINT1	I	78

Table U. JTAG Boundary Scan Signal Ordering (Continued)

PBGA Ball	Signal	Type	Position
N1	nEXTFIQ	I	79
L5	PE[2]/CLKSEL	I/O	80
N2	PE[1]/BOOTSEL1	I/O	83
M4	PE[0]/BOOTSEL0	I/O	86
T2	PD[7]/SDQM[1]	I/O	89
T3	PD[6/SDQM[0]]	I/O	92
N5	PD[5]	I/O	95
R3	PD[4]	I/O	98
T4	PD[3]	I/O	101
N6	PD[2]	I/O	104
R4	PD[1]	I/O	107
L7	PD[0]/LEDFLSH	O	110
T6	SSIRXFR	I/O	122
K8	ADCIN	I	125
R6	nADCCS	O	126
M8	DRIVE1	I/O	128
T8	DRIVE0	I/O	131
N8	ADCCLK	O	134
R8	ADCOUT	O	136
N9	SMPCLK	O	138
T9	FB1	I	140
M9	FB0	I	141
R9	COL7	O	142
L9	COL6	O	144
T10	COL5	O	146
K9	COL4	O	148
R10	COL3	O	150
N10	COL2	O	152
R11	COL1	O	154
M10	COL0	O	156
T12	BUZ	O	158
L10	D[31]	I/O	160
R12	D[30]	I/O	163
N11	D[29]	I/O	166
T13	D[28]	I/O	169
R13	A[27]/DRA[0]	Out	172
M11	D[27]	I/O	174
T14	A[26]/DRA[1]	O	177

Table U. JTAG Boundary Scan Signal Ordering (Continued)

PBGA Ball	Signal	Type	Position
N12	D[26]	I/O	179
R14	A[25]/DRA[2]	O	182
T15	D[25]	I/O	184
N13	HALFWORD	O	187
R16	A[24]/DRA[3]	O	189
P15	D[24]	I/O	191
M13	A[23]/DRA[4]	O	194
N16	D[23]	I/O	196
L12	A[22]/DRA[5]	O	199
N15	D[22]	I/O	201
L13	A[21]/DRA[6]	O	204
M16	D[21]	I/O	206
M15	A[20]/DRA[7]	O	209
K11	D[20]	I/O	211
L16	A[19]/DRA[8]	O	214
K12	D[19]	I/O	216
L15	A[18]/DRA[9]	O	219
K13	D[18]	I/O	221
J10	A[17]/DRA[10]	O	224
J16	D[17]	I/O	226
J11	A[16]/DRA[11]	O	229
J15	D[16]	I/O	231
J12	A[15]/DRA[12]	O	234
H16	D[15]	I/O	236
J13	A[14]/DRA[13]	O	239
H15	D[14]	I/O	241
H13	A[13]/DRA[14]	O	244
G16	D[13]	I/O	246
H12	A[12]	O	249
G15	D[12]	I/O	251
H11	A[11]	O	254
F15	D[11]	I/O	256
H10	A[10]	O	259
E16	D[10]	I/O	261
G13	A[9]	O	264
E15	D[9]	I/O	266
G12	A[8]	O	269
D16	D[8]	I/O	271

Table U. JTAG Boundary Scan Signal Ordering (Continued)

PBGA Ball	Signal	Type	Position
G11	A[7]	O	274
D15	D[7]	I/O	276
F13	nBATCHG	I	279
C16	nEXTPWR	I	280
F12	BATOK	I	281
C15	nPOR	I	282
E13	nMEDCHG/nBROM	I	283
B16	nURESET	I	284
B14	WAKEUP	I	285
D11	nPWRFL	I	286
A13	A[6]	O	287
F10	D[6]	I/O	289
B13	A[5]	O	292
E10	D[5]	I/O	294
B12	A[4]	O	297
D10	D[4]	I/O	299
A11	A[3]	O	302
G9	D[3]	I/O	304
B11	A[2]	O	307
A10	D[2]	I/O	309
F9	A[1]	O	312
B10	D[1]	I/O	314
E9	A[0]	O	317
A9	D[0]	I/O	319
D8	CL2	O	322
B8	CL1	O	324
E8	FRM	O	326
A7	M	O	328
F8	DD[3]	I/O	330
B7	DD[2]	I/O	333
A6	DD[1]	I/O	336
G8	DD[0]	I/O	339
B6	nSDCS[1]	O	342
D7	nSDCS[0]	O	344
A5	SDQM[3]	I/O	346
E7	SDQM[2]	I/O	349
F7	SDCKE	I/O	352
A4	SDCLK	I/O	355

Table U. JTAG Boundary Scan Signal Ordering (Continued)

PBGA Ball	Signal	Type	Position
D6	nMWE/nSDWE	O	358
B4	nMOE/nSDCAS	O	360
E6	nCS[0]	O	362
A3	nCS[1]	O	364
D5	nCS[2]	O	366
B3	nCS[3]	O	368
A2	nCS[4]	O	370

1) See EP7311 Users' Manual for pin naming / functionality.

2) For each pad, the JTAG connection ordering is input, output, then enable as applicable.

CONVENTIONS

This section presents acronyms, abbreviations, units of measurement, and conventions used in this data sheet.

Acronyms and Abbreviations

Table V lists abbreviations and acronyms used in this data sheet.

Table V. Acronyms and Abbreviations

Acronym/ Abbreviation	Definition
A/D	analog-to-digital
ADC	analog-to-digital converter
CODEC	coder / decoder
D/A	digital-to-analog
DMA	direct-memory access
EPB	embedded peripheral bus
FCS	frame check sequence
FIFO	first in / first out
FIQ	fast interrupt request
GPIO	general purpose I/O
ICT	in circuit test
IR	infrared
IRQ	standard interrupt request
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
LCD	liquid crystal display
LED	light-emitting diode
LQFP	low profile quad flat pack
LSB	least significant bit
MIPS	millions of instructions per second
MMU	memory management unit
MSB	most significant bit
PBGA	plastic ball grid array
PCB	printed circuit board
PDA	personal digital assistant
PLL	phase locked loop
p/u	pull-up resistor
RISC	reduced instruction set computer
RTC	Real-Time Clock
SIR	slow (9600–115.2 kbps) infrared
SRAM	static random access memory
SSI	synchronous serial interface

Table V. Acronyms and Abbreviations (Continued)

Acronym/ Abbreviation	Definition
TAP	test access port
TLB	translation lookaside buffer
UART	universal asynchronous receiver

Units of Measurement

Table W. Unit of Measurement

Symbol	Unit of Measure
°C	degree Celsius
fs	sample frequency
Hz	hertz (cycle per second)
kbps	kilobits per second
KB	kilobyte (1,024 bytes)
kHz	kilohertz
kΩ	kilohm
Mbps	megabits (1,048,576 bits) per second
MB	megabyte (1,048,576 bytes)
MBps	megabytes per second
MHz	megahertz (1,000 kilohertz)
µA	microampere
µF	microfarad
µW	microwatt
µs	microsecond (1,000 nanoseconds)
mA	milliampere
mW	milliwatt
ms	millisecond (1,000 microseconds)
ns	nanosecond
V	volt
W	watt

General Conventions

Hexadecimal numbers are presented with all letters in uppercase and a lowercase “h” appended or with a 0x at the beginning. For example, 0x14 and 03CAh are hexadecimal numbers. Binary numbers are enclosed in single quotation marks when in text (for example, ‘11’ designates a binary number). Numbers not indicated by an “h”, 0x or quotation marks are decimal.

Registers are referred to by acronym, with bits listed in brackets separated by a colon (:) (for example, CODR[7:0]), and are described in the EP7311 User’s Manual. The use of “TBD” indicates values that are “to be determined,” “n/a” designates “not available,” and “n/c” indicates a pin that is a “no connect.”

Pin Description Conventions

Abbreviations used for signal directions are listed in Table X.

Table X. Pin Description Conventions

Abbreviation	Direction
I	Input
O	Output
I/O	Input or Output

Ordering Information

Model	Temperature	Package
EP7311M-IBZ	-40 to +85 °C.	256-pin PBGA, 17mm X 17mm

Environmental, Manufacturing, & Handling Information

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
EP7311M-IBZ	260 °C	3	7 Days

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

Revision History

Revision	Date	Changes
PP1	NOV 2003	First preliminary release.
F1	AUG 2005	Updated SDRAM timing. Added MSL data.
F2	MAR 2011	Removed all lead-containing device ordering information. Added EP7311M-IBZ.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

To find the one nearest to you go to www.cirrus.com